PULSE DENSITY MODULATED SOFT SWITCHING CYCLOCONVERTER

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Committee Membership Page

Title: Pulse Density Modulated Soft Switching Cycloconverter

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Abstract

Pulse Density Modulated Soft Switching Cycloconverter

Jesse Adamson

Single stage cycloconverters generally incorporate hard switching at turn on and soft switching at turn off. This hard switching at turn on combined with the slow switching speeds of thyristors (the switch of choice for standard cycloconverters) limits their use to lower frequency applications.

This thesis explores the analysis and design of a pulse density modulated (PDM), soft switching cycloconverter. Unlike standard cycloconverters, the controller in this converter does not adjust thyristor firing angles. It lets only complete half cycles of the input waveform through to the output. This allows and requires a much greater frequency step down from the input to the output. The advantages, shortcomings and tradeoffs of this topology are explored as this converter is designed, built and tested.

The resulting cycloconverter has many deficiencies, but proves the concept of the PDM soft switching technique. Cases for further improvement and study are outlined. In the end, this converter shows much promise for applications requiring a high step down in frequency, as well as where the lower electromagnetic interference (EMI) of soft switching may be beneficial.

Acknowledgments

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Thanks are also due to John Dunning for greatly aiding in my thesis topic decision process. On many occasions you have bestowed enlightening information in the fields of electric vehicles, batteries, politics and general advice. I appreciate your encouragement in pursuing this thesis topic.

Taufik deserves much acknowledgement as well. It was in your power electronics classes that I gained the skills and ideas that led me to, and allowed my design of the soft switching cycloconverter. Your positive attitude and obvious hard work in motivating us students to reach our maximum learning potential continually inspires me. I am so glad you were able to advise me on this thesis. It has been a pleasure working with you and I greatly appreciate your tolerance of my last minute attitude.

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Chapter 1. Introduction

Many years have passed since the epic battle of Tesla vs. Edison and the birth of the modern electric grid. [1] Over the years electricity has been integrated deeply and increasingly into our lives. As technology has advanced, electrical devices have greatly expanded in their power requirements. To facilitate power conversion to meet these requirements, various techniques have been developed and employed into what is now referred to as the field of Power Electronics.

Today many electrical loads use power electronics. These include cell phones, computers, stereos, televisions and various home appliances. It is common for these devices to use power electronics extensively. For example, different circuitry in various parts of a computer requires different voltage and current levels that must be regulated by advanced power electronics. Cars use power electronics as well. Besides their computer and complex support systems, the alternator uses power electronics to convert its power from alternating current (AC) to direct current (DC) and regulate its output voltage.

Another important use of power electronics is in newer portable generators. These generators are improving efficiency and reducing noise output by running at variable speeds and using power electronics to convert their output to line frequency such as 50 Hz or 60 Hz and regulate their voltage. Many large generators on wind turbines use this technique as well. Modern trains and ships employ a similar technique in their series hybrid drives. This involves a high

efficiency gas turbine engine running a high frequency generator that, using power electronics, is variably fed into an electric motor to power the craft.

The utility grid is evolving through the use of power electronics too. With advanced in solid state switch technology, grid regions that are not synchronized or running at different frequencies can be tied together using high voltage DC transmission lines. These DC lines utilize power electronics converters that can regulate the direction and flow of power. For very long distance transmission, DC lines are more efficient and require less material to build than comparable AC transmissions lines.

Power electronics create and adjust voltage levels in the traditional way using AC generated magnetic fields. The advancement is in techniques to adjust voltage and current levels as well as convert between DC and AC of various frequencies. With power electronics, solid state switches are used to generate AC signals at high frequencies. The higher frequencies are often needed to reduce magnetic component size and improve efficiency. These requirements are exemplified in ship and aircraft power systems which typically run at 400Hz. AC signals may also be variably stepped down in frequency to turn heavy machines such as those found in wind turbines and large cruise ships. There are many standard methods or topologies to accomplish these AC to AC conversions. The cycloconverter is one commonly used AC-AC conversion technique that lowers the frequency, and can also change the number of phases of electrical power as it is being transferred from one power bus to another.

In this thesis, a new modulation technique is applied to a standard single phase cycloconverter. The technique attempts to improve efficiency by implementing soft switching. This provides several potential benefits as well as tradeoffs. The design is simulated and prototyped to explore its strengths, weaknesses and potential for further development and implementation into power systems.

Chapter 2. Background

The simplest cycloconverter is the single phase to single phase topology. This is implemented with four bi-directional switches in an H-bridge configuration as shown in Figure 2-1. In this configuration, the switches are operated in pairs. Switching on only S1 & S4 causes the current through the load to flow in forward polarity with AC-IN, while switching on only S2 & S3 causes the current to flow in reverse polarity with AC-IN. This operation allows current to flow either direction through the load, for any given polarity of the AC-IN source. The switches can, therefore, be activated in such a way that the average or filtered output waveform is the desired wave shape (sinusoidal) and frequency.

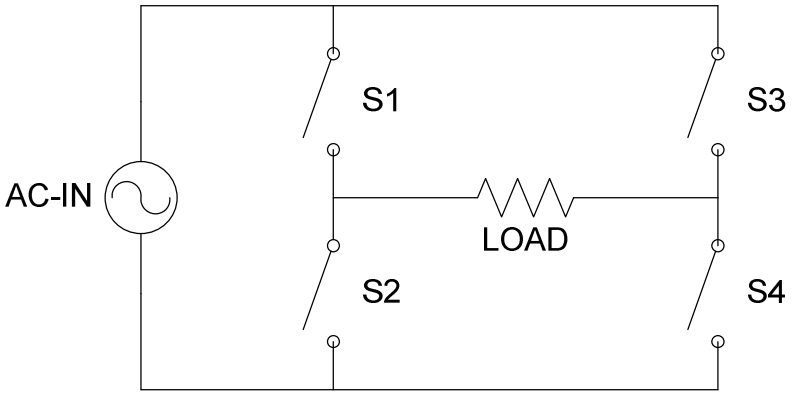

Figure 2-1. Single Phase Cycloconverter with Bidirectional Switches

Standard power Field Effect Transistors (FET's), and Insulated Gate Bipolar Junction Transistors (IGBT's) are unipolar. That is, they only block and

allow current flow in one direction. For this reason, they are not viable realizations of S1 through S4. Triacs are standard bidirectional switches sometimes used for small scale cycloconverters. They are not currently available for large current applications.

Standard transistors can be arranged to form a bidirectional switch as seen in Figure 2-2. This can work for medium applications like electric vehicles and industrial motor drives. Their advantage is the high switching speeds of standard FET's or IGBT's. Their disadvantage is the extra voltage drop created by the diode in series with the switch. This diode is essential for two reasons: first to create a path for current to flow around which ever transistor happens to be reverse biased, and second to prevent the transistor form being reverse biased with significant voltage.

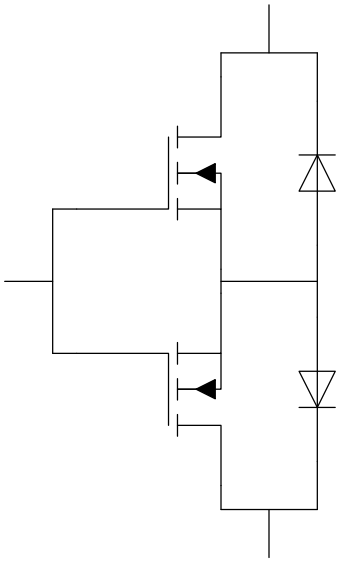

Figure 2-2. Bidirectional Transistor Switch [5]

FET's have an inherent diode in the reverse direction making them incapable of reverse blocking. This inherent diode is poor quality, however, so an additional fast diode is usually designed into the silicon substrate as well. If this is the case, then no additional discrete diodes are required in the design.

IGBT's, unlike FET's, are capable of reverse blocking. However, their reverse blocking capability is usually a small fraction of their forward blocking capability. For this reason, most power IGBT's are produced with an additional diode as well. There are new reverse blocking IGBT's capable of high reverse voltages, but these are currently several times as expensive as standard IGBT's of the same forward ratings. As their price comes down, these reverse blocking IGBT's should provide a viable alternative to the current standard.

The current standard switch for cycloconverters is the thyristor. This is a three terminal device, like standard transistors. Unlike standard transistors, however, thyristors have very high reverse voltage blocking capabilities. Also, unlike transistors, thyristors cannot be turned off. They are semi-controllable switches that are turned on by a pulse of current injected into their gate and pulled out of their cathode. Once the thyristor switches on, it continues to conduct electrical current until it is reverse biased. At this point it automatically resets itself and will not turn on until it is forward biased and receives another gate current pulse. This semi-controllability presents a problem in many applications, but is no problem in cycloconverters because the AC input automatically reverse biases the thyristors for half of each cycle.

Another differentiating feature of thyristors is their ability to handle huge currents, some upwards of several thousands of amps. They are also priced comparably less than high current transistors. Their disadvantage, besides semi-controllability, is their much slower switching speeds compared to FET's and even IGBT's. This is one reason that cycloconverters are usually run at lower frequencies than switch mode DC-DC converters and transistor inverters.

Like transistors, thyristors are unidirectional. For this reason, thyristor cycloconverters require twice as many switches as a bidirectional switch cycloconverter. This can be seen in Figure 2-3.

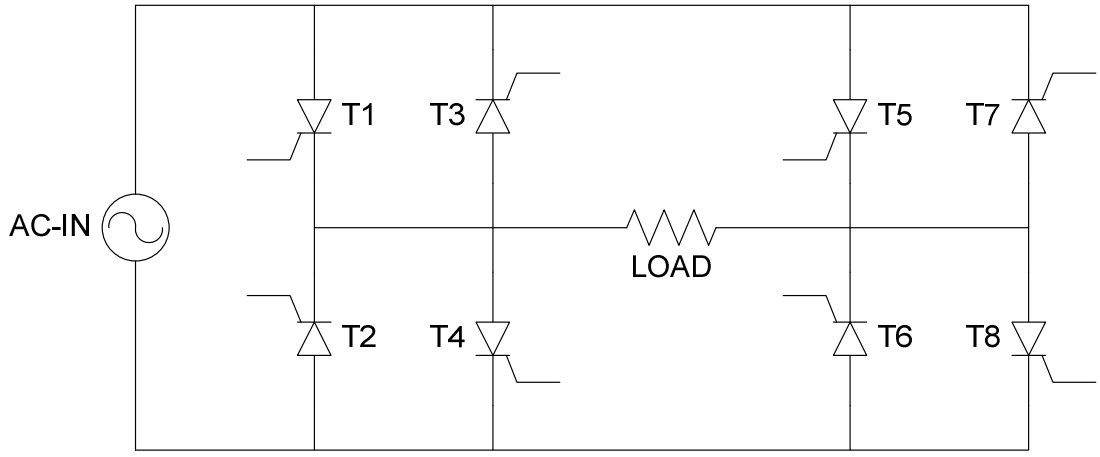

Figure 2-3. Single Phase Cycloconverter with Unidirectional Switches

Though the standard single stage cycloconverter has been around for many years and remains in mainstream use in many applications today, there are many possibilities for improvement on this topology. These range from new types of switches to new switching control algorithms.

One potential improvement from a control standpoint is soft switching. Soft switching is turning the switch on or off with zero voltage or current across the switch. There are four elements of soft switching, some combination of which must be utilized for a converter to qualify as soft switching. They are zero voltage switching (ZVS) at turn on or turn off and zero current switching (ZCS) at turn on or turn off.

Since power is current times voltage, if either current or voltage across the switch is zero during the turn on or turn off transitions, the respective switching loses are eliminated. In actuality, it is not possible for the current or voltage to be exactly zero for the entire turn on and turn off transition. For this reason, soft switching cannot completely eliminate, but can only reduce switching losses in real world applications.

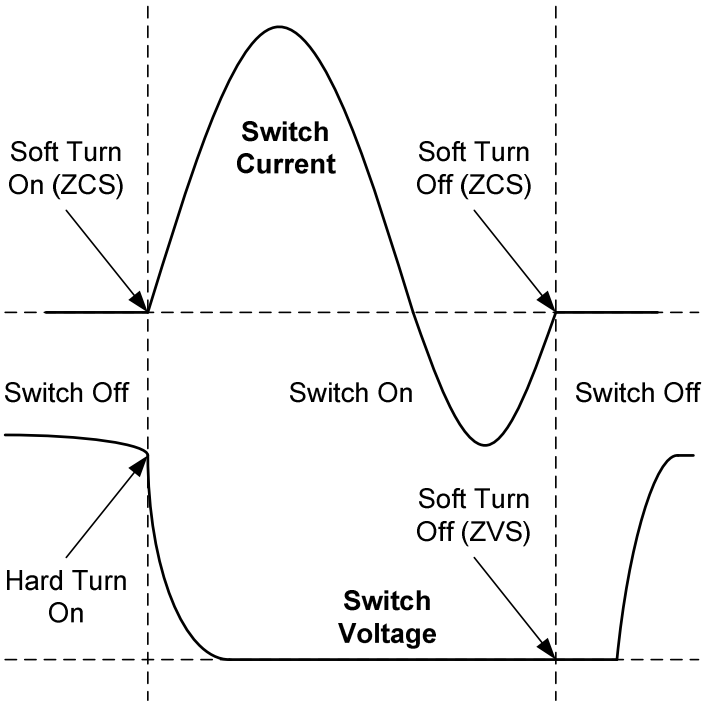

Figure 2-4. A Soft Switching Trajectory

To better understand soft switching, it is important to take a look at its counterpart, hard switching. Hard switching is the standard for most power converters today. This is due to its simplicity, durability and heritage. In hard switching, switches are turned off with all or a significant portion of the supply voltage across the switch. Therefore, during the transition current is flowing through the partially activated switch. This voltage and current converts electrical power to heat in the switch, which must be dissipated.

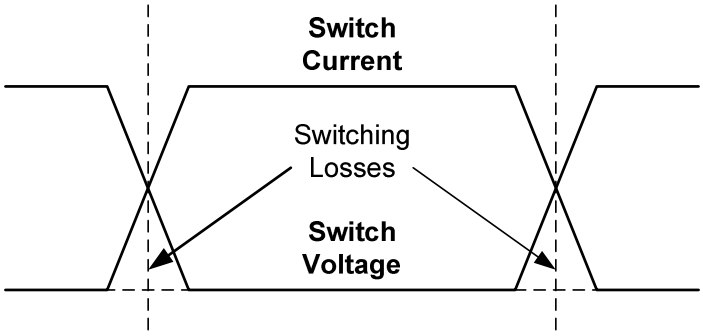

Figure 2-5. A Hard Switching Trajectory

To facilitate soft switching, the voltage across the switch and/or current through the switch must propagate in such a way as to automatically cross the zero axes so the switch can be turned off softly. In DC-DC converters this is done by including a resonant tank after the switch. This resonant tank causes the voltage and current to oscillate when the switch is turned on. This in turn causes a pulse to flow through the switch, after which the voltage and/or current is reduced to zero and the switch is turned off. These DC-DC converters are known as resonant converters.

In cycloconverters, the AC input power provides the oscillation through the zero current and voltage crossings, so no resonant tank is required. In addition, soft turn off is inevitable in a standard cycloconverter using thyristors. This is because the thyristors only turn off when reverse biased, which happens automatically just after the zero crossing when the current through and voltage across them is very low. Turn on in a standard cycloconverter, however, is controlled by injection of gate current. This is performed by a controller using a reference waveform.

The controller's job is to make the output waveform track the reference by adjusting the switching point of the thyristor relative to the input waveform. This relative switching point to the input is referred to as the thyristor firing angle. When the firing angle is near the beginning or towards the end of the waves' forward half cycle (forward relative to the thyristor), the voltage is less and so the switching loss is less. When the firing angle is in the middle of the forward half cycle, the switching loss is more. Either way, the thyristor exhibits hard switching at turn on.

There is one easy way to achieve soft switching at cycloconverter turn on. That is to turn the switch on at the beginning of the forward half cycle and let the entire pulse through. This is shown in Figure 2-6.

Because thyristors are unidirectional, the thyristor gate can actually be charged before the beginning of the forward half cycle. For example, in the middle of the preceding reverse half cycle. This could help the thyristor turn on as soon as possible when it becomes forward biased.

The drawback of letting only full pulses through is the requirement of a much higher input to output frequency ratio and/or more output voltage filtering. This increased input frequency, however, has a much lighter impact on efficiency due to the soft switching. This is especially advantageous considering the slow switching speed of thyristors.

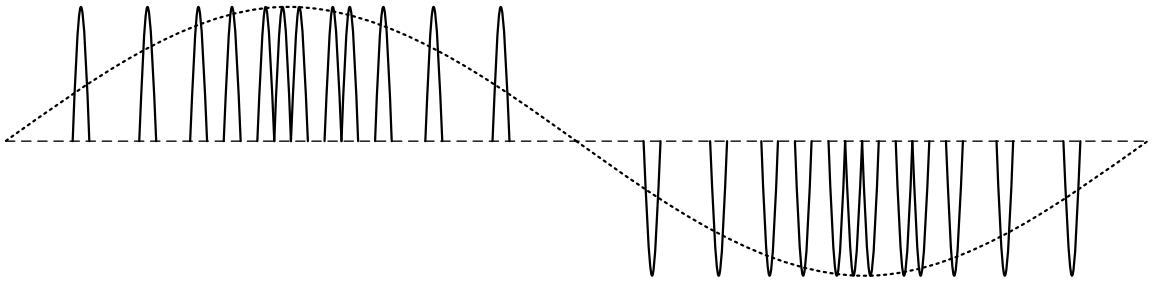

Figure 2-6. Monopolar Pulse Density Modulation

This idea of letting pulses through in discrete time to represent an output signal was developed under the formal name of Pulse Density Modulation (PDM). The origins are in analog to digital converters, namely delta sigma converters. In PDM, a digital pulse train is passed through an analog filter to produce a continuous waveform. This method is in contrast to popular modulation techniques in power electronics like Pulse Width Modulation (PWM) and Pulse Frequency Modulation (PFM). These three are compared and contrasted in Table 2-1.

Table 2-1. Comparison of Modulation Techniques

	PWM	PFM	PDM
On Time	Continuous	Continuous/Discrete	Discrete
Off Time	Continuous	Discrete/Continuous	Discrete
Frequency	Discrete	Continuous	Discrete

Along with each modulation technique are the ideas of monopolar and bipolar switching. Bipolar switching is the simplest. In Bipolar, the output has two levels, high and low or maximum positive and maximum negative. For the output to be in the middle (zero voltage for the typical sine wave) the output runs at 50% duty cycle, switching back and forth between high and low. For monopolar, on the other hand, the output has three levels: high, low and middle. This means that the output is never negative when the reference is positive and vice versa. This method requires more complex controls, but less output filtering.

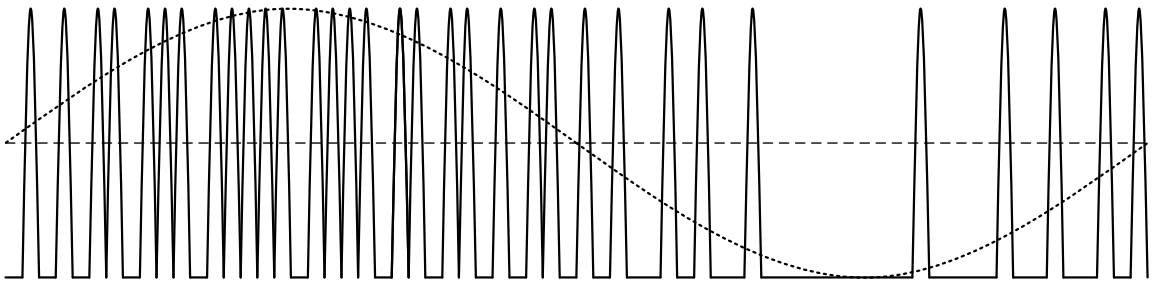

Figure 2-7. Bipolar Pulse Density Modulation

The simplest realization of PDM is the single bit delta sigma converter control loop shown in Figure 2-8. Delta sigma converters can have many bits, but for a single PDM line, only one bit is needed. In the delta sigma, a reference waveform is added to a negative feedback signal and fed into an integrator. The output of the integrator is compared to a threshold. After the reference waveform causes the integrator to rise above the threshold, the converter outputs one discrete pulse. This pulse is negatively fed back to the initial summing junction, reducing the integrator. This regulation produces an output pulse train whose integrated area is linearly proportional to the reference wave's integrated area. This output pulse train is then run through a low pass filter to reconstruct the reference wave.

The integrator can be realized with a standard op-amp in integrating configuration, that is, with a capacitor in its negative feedback path. The discrete pulse output can be handled by a one bit analog to digital inverter. This is realized using a comparator and a D flip flop.

This is an example of bipolar switching. To make this monopolar switching would require two comparators; one for a high threshold and one for a low. It would also require the ability to output two discrete pulses, one positive and one negative, as well a feedback signal from each to the integrators input summing junction. Implementing this requires two comparators, one for the high threshold and one for the low.

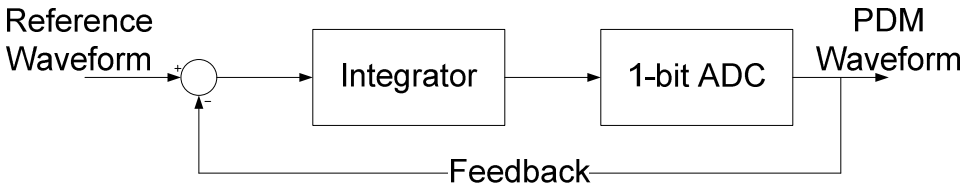

Figure 2-8. Delta Sigma A/D Converter [2]

The idea of a cycloconverter utilizing soft switching based on pulse density modulation has been around for several years. A 2003 paper from Xi'an University in China [4] lays out this exact approach for a three phase cycloconverter. This converter uses a DC input inverted through a resonant converter whose AC output is fed into a soft switching cycloconverter. This paper points out that if the soft switching frequency can be increased high enough above a comparable hard switching frequency, and the switching loss adequately reduced, then the output could actually require less filtering compared to a hard switching converter. This paper focused mostly on modeling the cycloconverter mathematically, with little simulation and no prototyping.

There are three very similar papers, essentially different revisions, from Kobe University, Japan dating back to 1991 [6], [7], [8], that utilize a PDM soft switching cycloconverter as well. These papers also use various resonant converters as the input to the cycloconverter. Their target application is power conditioning, though one paper mentions straight power conversion as well. They did build the hardware and had some interesting results for different non-linear loads. Their converter responded adequately to inductive loads, but had trouble

with rectified loads going to a capacitor. They did not show un-rectified capacitive loads.

Additional variants on the soft cycloconverter include a paper from the University of Tabriz, Iran [5], which uses an isolated input to the cycloconverter. This topology employs a center tapped transformer and two bidirectional switches, allowing half of the transformer output voltage for the high half cycle and half for the low half cycle. Another similar converter also using bidirectional switches is described in a paper from University of Illinois [9], which targets Solid Oxide Fuel Cells (SOFC's). They boast a prototype efficiency of 91% for their whole system which consists of a resonant boost converter, a high frequency inverter and a cycloconverter. They describe soft switching in the boost converter, but it is unclear whether the cycloconverter is utilizing this as well. If not, adopting this approach could potentially benefit their design.

Another paper from the Institut de Genie Energetique, France [10], describes the use of a soft switching cycloconverter for electric vehicle (EV) applications. Their design uses one input to two cycloconverters, presumably for two hub motors on a two wheel drive EV. The novelty in their design is IGBT based bidirectional switches in full bridge single phase to three phase configuration. This results in six bidirectional switches per cycloconverter.

Other applications described in [11] and [12] include high frequency soft switching cycloconverters for induction heaters and magnetrons. Induction heaters are used in many industries including cooking, cap sealing and foundry. Magnetrons generate microwaves, mainly in microwave ovens. These two

applications are suggested by roughly the same group of people from various universities in Korea and Japan. Their topology has a significantly reduced part count implemented using transistors in bi-directional switch groups.

Though some research has been done into this niche of soft switching cycloconverters, there is certainly more research needed to advance their practical application. Several applications have been identified where high frequency input to low frequency output high efficiency cycloconverters could thrive. In this thesis, in an attempt to further improve cycloconverter technology and improve soft switching cycloconverter credibility, a full bridge, soft switching, thyristor based, grid frequency, PDM controlled cycloconverter is proposed, designed, built and investigated.

Chapter 3. Design Requirements

3.1. Design Goals:

The proposed cycloconverter in this thesis is based on a single phase input, single phase output topology. This is the simplest topology and is chosen for proof of concept in exploring the basic properties of the pulse density modulated soft switching technique proposed. The output frequency is set to 60 Hz for compatibility with standard United States line frequency. 5 KHz is used for the input frequency because it is the limit of the power supply in our lab. This is high enough to allow reasonable filtering from the proposed cycloconverter and low enough to be within the frequency limits of the high frequency power supplies in the lab.

The input will use a fifty volts peak AC sine wave. This voltage is high enough to allow reasonable power transfer and low enough to be around standard safety limits to reduce chances of electrical shock. The peak unfiltered output voltage will be the same as the input, minus the small voltage drop across the two thyristors in series with the load. For the filtered output, the peak voltage will be much less, and will depend on the average pulse density, which can be adjusted in the controller. The output current will shoot for around ten amps at full load. This results in approximately a 350 W cycloconverter.

An open loop control is used to map the converter output to the reference voltage. This converter does utilize an internal feedback loop; however, there is no voltage or current sensing on the actual converter output. For this reason, the

converter has no line regulation. However, the load regulation will be tested from roughly 10% to 100% of load.

There is no input filtering on the converter. To explore the quality of power drawn by the cycloconverter, the input power factor (PF) will be measured. The output necessarily employs an LC filter with a purely resistive load. The filtered output harmonic spectrum and total harmonic distortion (THD) will be tested.

Overall converter efficiency will be mapped over varying loads. Loads will vary from one to ten amps (10% to 100%). Power resistors will be combined in different series/parallel combinations to simulate varying loads. Effects of temperature, humidity and other environmental factors will be ignored.

Table 3-1. Summary of Design Requirements (TBD is to be determined)

Parameter	Input/Line	Output/Load
Number of Phases (ϕ)	1	1
Frequency (Hz)	5000	60
Voltage AC sine (V-Peak)	50	TBD
Full Load Current AC sine (A-RMS)	N/A	10
Regulation (%)	N/A	TBD
Power Factor	TBD	1
Voltage Frequency Response	N/A	TBD
Total Harmonic Distortion (%)	N/A	TBD
Efficiency (%)	TBD	

3.2. Test Procedure:

The peak output voltage will be lower than the peak input voltage due to switching duty cycles and switching losses. The duty cycles are adjustable by adjusting the reference voltage, thereby increasing the average output pulse density. These are expected to max out and produce distortion of the output waveform well before the output peak voltage reaches the input peak voltage. With the soft switching reducing transient losses, total switching losses should be predominantly due to forward voltage drops. There are two thyristors per current path and therefore two forward voltage drops. The peak output voltage will be measured using an oscilloscope.

Load regulation is determined by varying the load with the input set to its nominal value:

$$\text{Load Regulation} = \frac{V_{O(LOW-LOAD)} - V_{o(HIGH-LOAD)}}{V_{O(NOM)}} \times 100\% \qquad (3\text{-}1)$$

Efficiency and power factor will be measured using a power meter. Efficiency is calculated using equation (3-2). Frequency response and THD will be recorded using power quality analyzer such as the PowerSight or Fluke 43B.

$$\text{Efficiency} = \frac{P_{OUT-AVERAGE-MEASURED}}{P_{IN-AVERAGE-MEASURED}} \times 100\% \qquad (3\text{-}2)$$

$$\text{THD} = \frac{P_{TOTAL} - P_{FIRST-HARMONIC}}{P_{FIRST-HARMONIC}} \qquad (3\text{-}3)$$

$$PF = \frac{\text{Real Power (W)}}{\text{Apparent Power (VA)}} = \frac{P}{S} \tag{3-4}$$

3.3. Design Details:

The soft switching cycloconverter design can be broken down into several blocks: the load, the filter, the thyristors, the drivers, the controller logic block and the controller analog block as illustrated in Figure 3-1. The main input power flows through the thyristors. They are triggered by the drivers via control lines from the logic block. The logic block decides which thyristors to turn on by comparing signals in the controller analog block.

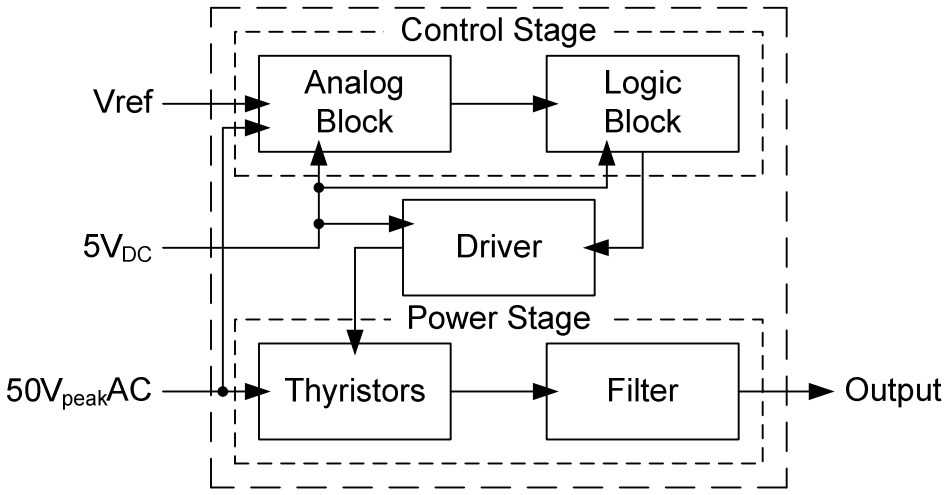

Figure 3-1. Soft Switching Cycloconverter Block Diagram

Though the power and signals flow from left to right, the design actually starts with the single phase cycloconverter topology embodied in the Thyristor block. From here the design moves backwards to the drivers needed to fire the thyristors. The controller is then designed to operate the drivers. The controller is broken into analog and digital subsections because the design of these blocks is significantly different. The filter is a large CL low pass that may stand external to the main circuit board due to its size. The load will consist of various wire wound power resistors.

The proposed cycloconverter design requires a quick look at how this topology functions. Cycloconverter operation requires that each input line be connectable to each output phase pair in both directions. This can be thought of as H-bridges with tops and bottoms connected to inputs of the converter, and centers connected to outputs. There must be an H-bridge for every combination of input pairs to connect to every combination of output pairs. This requires the following total number of switches:

$$\#\ \text{Switches} = \#\ \text{Lines In} * \#\ \text{Phases Out} * 4 \qquad (3\text{-}5)$$

By this formula, a single phase to single phase cycloconverter has two lines in, one phase out equating to eight switches. One way to visualize and draw these switches is in H-bridge configurations. In this instance, the bridges are facing in opposite directions stacked on top of each other sharing the load connected at their centers. These H-bridges are seen in Figure 3-2 as thyristors

T3, T2, T7, T6 in the upward facing bridge and thyristors T1, T4, T5, T8 in the downward facing bridge.

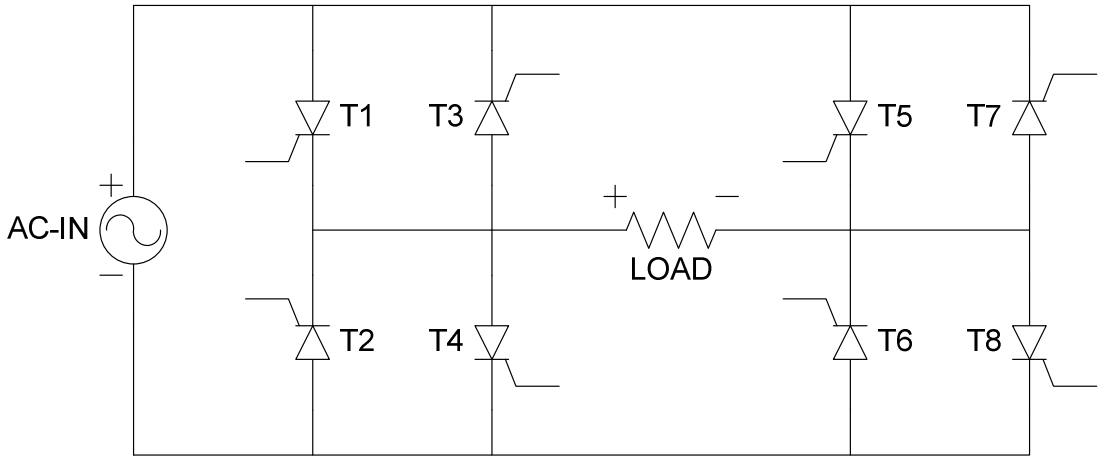

Figure 3-2. Single Phase Cycloconverter

Thyristors turn on when a current pulse travels in through their gate and out through their cathode. This pulse can come from any source. However, the simplest is to pull it from the thyristors anode. When the thyristor gate is connected to the anode, the thyristor acts like a diode. The drawback of this technique from a soft switching standpoint is that the thyristor must be forward biased before current can start flowing into the gate. This is not a significant problem because the thyristor needs to be forward biased to turn on anyway. A separate pulse starting earlier in the cycle however, may help the thyristor turn on slightly faster or more softly. In this thesis the first and simpler option of shorting the gate to the anode will be used.

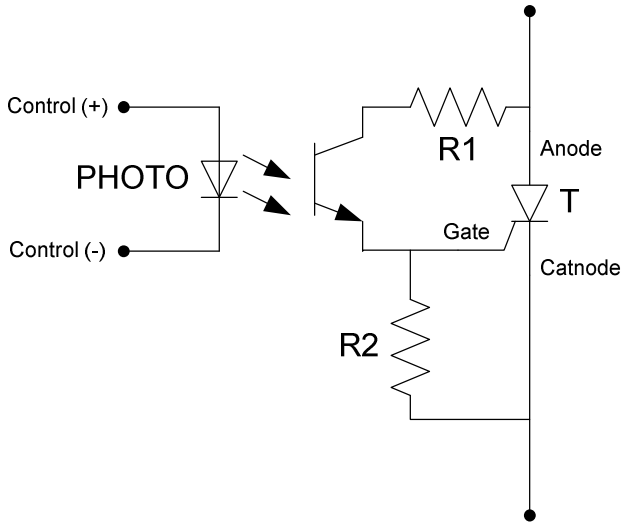

Figure 3-3. Thyristor Driver

In this thyristor driver circuit, the control signal activates a bipolar junction transistor (BJT) style photocoupler that feeds current from the thyristor anode through the thyristor gate. R1 limits the current pulse and R2 ensures the gate stays low when the photocoupler is off. R1 must be sized to turn on the thyristor as soon as possible, yet keep current at a safe level at the 50V peak of the input supply. R2 must be significantly larger than R1 so it does not draw much of the pulse current, yet small enough to be effective. For our purposes, R1 was determined experimentally and set to 82 Ω and R2 was set to 10 KΩ.

The thyristors are activated in pairs and therefore arranged into four switch groups. Each switch group allows current to flow in one direction through the load from one half cycle of the AC source. Although each thyristor has its own driver, each switch group is activated by a single control signal. This means each control signal connects to two drivers.

The control signals are named based on the thyristors they drive, referenced from Figure 3-2. These are shown in the first column of Table 3-2. Each control signal is designed to let one pulse (one half cycle of the input waveform) through to the output. Each signal can only map a signal input polarity to a single output polarity, thereby requiring four control signals to control the four input polarity to output polarity combinations.

Table 3-2. Control Signals from Logic Block to Thyristor Drivers

Control Signal	Thyristors	Pulse Mapping
to18	T1 & T8	Positive Input Pulse to Positive Output Pulse
to27	T2 & T7	Negative Input Pulse to Positive Output Pulse
to36	T3 & T6	Negative Input Pulse to Negative Output Pulse
to45	T4 & T5	Positive Input Pulse to Negative Output Pulse

To determine how to activate these control signals, it is important to take a look at the required input signals. Inputs include chip power, a reference sine wave and the main high frequency AC power source. These inputs will be compared along with the PDM integrator and transformed into discrete signals that the logic block will use to decide when to fire which thyristors.

In order to decide when to fire the thyristors, the Analog Block starts by comparing several values and encoding them in digital signal lines. First the voltage polarity of the high frequency input is needed. This signal is named “resp”. It will be high when the high frequency source is in its positive half cycle,

or resonating positively. This signal is used to make sure thyristors are reverse biased when their drivers are activated and deactivated so they are ready to turn on as soon as they start to become forward biased. This ensures soft turn on. The drivers can switch off when the thyristors are forward biased because this does not turn off the thyristors. They continue to conduct until reverse biased.

Likewise the reference polarity will be encoded in the “refp” signal. This signal will be positive when the reference is positive. It will be used to ensure that output pulse polarity always matches reference polarity. This is necessary for the converter switching to be classified as monopolar.

Additionally, a “CLK” signal will be needed to determine exactly when to turn the thyristors on and off in their respective half cycles. The clock should transition somewhere in the middle of each half cycle. This signal, along with “resp” and “refp” hold all the required information to line up the output pulses.

The only needed information remaining is when to emit a pulse. This is where the PDM integrator comes in and requires two signals because the switching scheme is monopolar. The “intGreater” signal is triggered high when the integrators output voltage rises above the high threshold, therefore requiring a positive output pulse that is negatively fed back to the integrator to bring it back down. Likewise, a high “intLess” signal signifies the integrator output voltage dropped below the low threshold requiring a negative output pulse that is negatively fed back to bring it back up. These signals are summarized in Table 3-3.

Table 3-3. Signals from Analog Block to Logic Block

resp	Positive for main input voltages positive half cycle
refp	Positive for reference voltages positive half cycle
CLK	Rising edge around the middle of each main input half cycle
intGreater	Positive when a positive output pulse is needed
intLess	Positive when a negative output pulse is needed

The Logic Block receives these five signals and outputs six signals. Four of the outputs are the driver control signals listed in Table 3-2 and two signals are feedbacks to the Analog Block. The two feedback signals are shown in Table 3-4 as OR gated combinations of the control signals.

Table 3-4. Feedback Signals from Logic Block to Analog Block

lastPulseP	to18 OR to27
lastPulseN	to36 OR to45

The logic block is designed by looking at each of the four control signals independently. The thyristor diagram in Figure 3-2 is used along with the input signals to the Logic Block in Table 3-3 to determine this logic flow. The “CLK” signal specifies when the driver control signals can change. This implies that the control signals have memory, which will be implemented in the form of a D flip

flop for each. Therefore, the “CLK” signal triggers the clock input of the flip flops only and is not found in the logic equations describing to18, to27, to36 and to45.

Starting with the first row of Table 3-2 it is seen that signal to18 maps a positive input pulse to a positive output pulse. This should happen when the input is in its negative half cycle (resp is low), the reference is in its positive half cycle (refp is high) and a positive pulse is required (intLess is high). The other signals are found similarly:

$$to18 = \overline{resp} \cap refp \cap \text{int}\,Greater \tag{3-6}$$

$$to27 = resp \cap refp \cap \text{int}\,Greater \tag{3-7}$$

$$to36 = resp \cap \overline{refp} \cap \text{int}\,Less \tag{3-8}$$

$$to45 = \overline{resp} \cap \overline{refp} \cap \text{int}\,Less \tag{3-9}$$

The control signals are easily implemented using standard NOT gates along with three input AND gates. The four AND gates output to the four D flip flops. These control signals outputted from the flip flops connect to the gates of intermediate metal oxide semiconductor field effect transistors (MOSFETS) that drive the respective photodiodes on the thyristor driver photocouplers. Two OR gated are also implemented as described in Table 3-4 whose outputs are the feedback signals to the integrator: “lastPulseP” and “lastPulseN”.

These feedback signals are combined with the reference in a summing junction at the integrators input. The summing junction and integrator can be implemented using a standard op-amp with a capacitor in its negative feedback

path. In this case, with the opamp using its inverting configuration, the output signals “intGreater” and “intLess” must be swapped to maintain sign consistency.

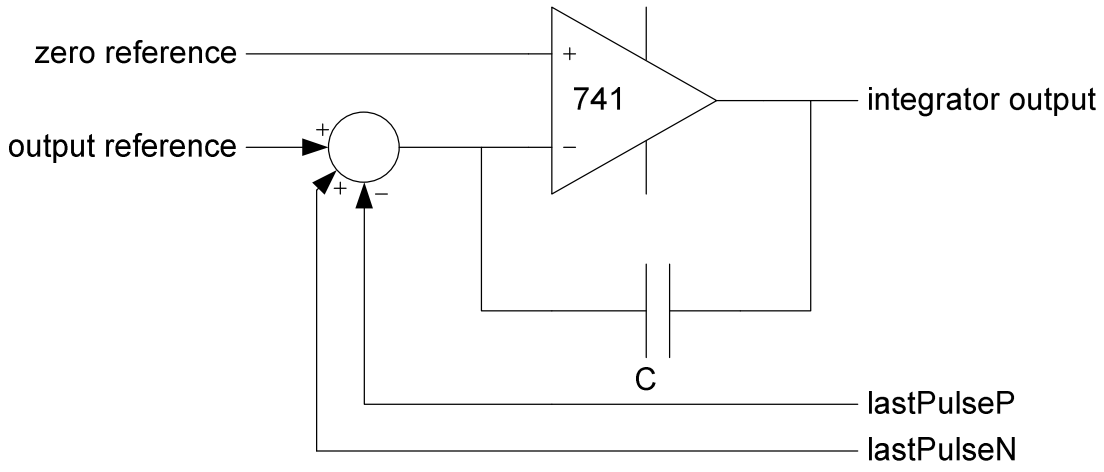

Figure 3-4. PDM Integrator

The comparisons made by the analog block use standard comparators. For the high voltage signals, resistor dividers are implemented. There are several ways to get “CLK”. A simple solution it to use a capacitor with a high value shunt resistor to hold the negative terminal of the comparator close to the peak of the input source. This capacitor is charged from the source resistor divider through a diode that prevents discharge. The positive comparator terminal is connected directly to the source resistor divider. The shunt resistor allows a slight discharge of the capacitor while the diode is reverse biased, keeping the comparator negative terminal voltage just below the peak voltage of the divided rectified sine wave. For a short time near the peaks of the rectified wave, the positive terminal

voltage exceeds the negative terminal voltage (capacitor voltage) due to the diode drop. This sends the comparator output high generating the “CLK” pulse.

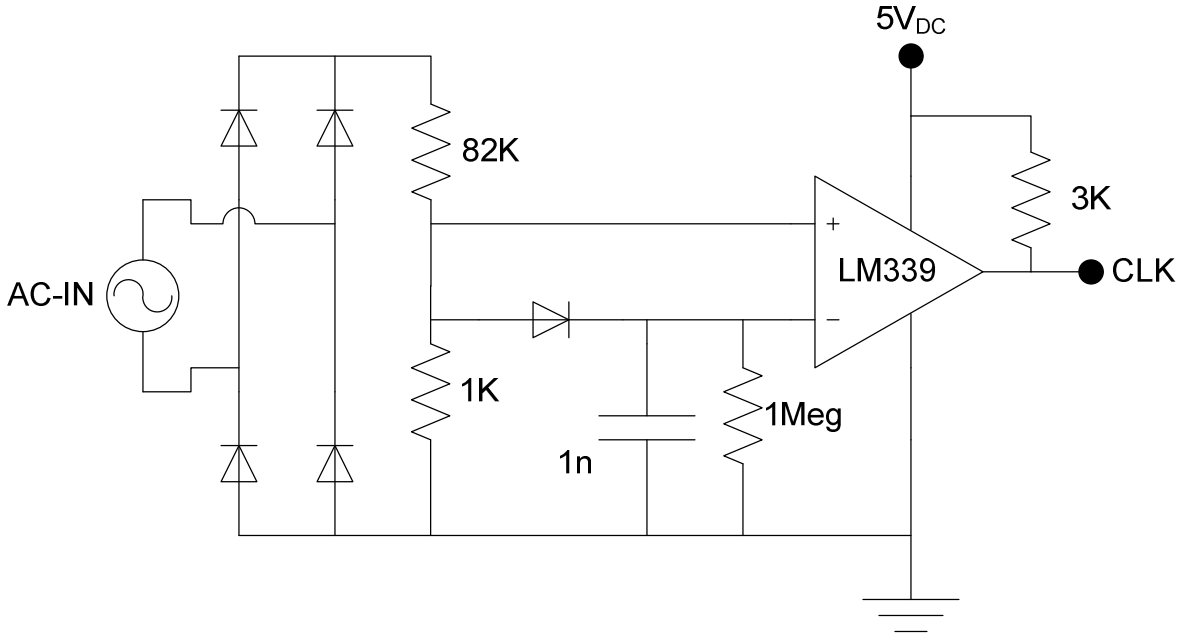

Figure 3-5. Generating the “CLK” Signal

The output filter is all that’s left to design, since a purely resistive load will be used. The standard output filter for inverters is an LC low pass. This is configured with the inductor in series with the load, blocking high frequencies, and the capacitor parallel to the load, shorting high frequencies to ground. This presents a problem with the cycloconverter, however, because when all the switches are off, there is no path for the inductor to discharge. For this reason, the L and C must be swapped to form a CL filter. This allows the inductor to pull current from the capacitor when the thyristors are off.

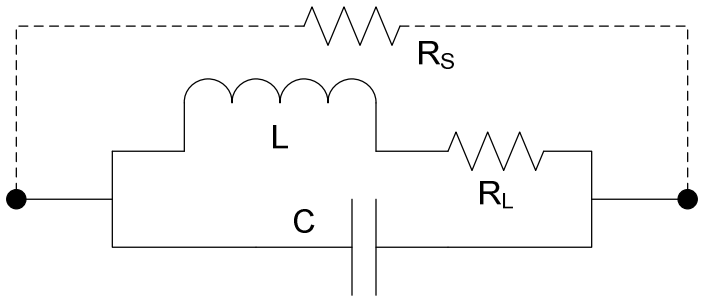

Figure 3-6. CL Filter with Load and Source Resistance

When designing a low pass filter, start with the transfer function [3]. Then the magnitude is found by multiplying the transfer function by its complex conjugate. Next, the desired cutoff frequency (ω_C) is chosen. This is usually specified to be one hundred times less than the switching frequency, however, in this design that would be 50 Hz. Since 50 Hz is less than the output frequency, the cutoff frequency must be higher and will be chosen as 300 Hz. From here, write a new equation by setting the magnitude equal to -3 db times its original DC value (half power). Then select a value for either L or C and use this equation to solve for the other.

Alternatively, this second order transfer function can be rearranged into standard form. This gives the natural frequency (ω_n) by inspection, which in the case of a low pass filter is equivalent to ω_C.

$$H(s) = \frac{K}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{3-10}$$

$$H(s) = \frac{R_L}{LCR_S s^2 + s(L + CR_L R_S) + (R_L + R_S)} \tag{3-11}$$

$$\Rightarrow \frac{\frac{R_L}{LCR_S}}{s^2 + s\frac{(L + CR_L R_S)}{LCR_S} + \frac{(R_L + R_S)}{LCR_S}} \tag{3-12}$$

$$\omega_C^2 = \omega_n^2 = \frac{R_L + R_S}{LCR_S} \tag{3-13}$$

$$LC = \frac{R_L + R_S}{\omega_C^2 R_S} \tag{3-14}$$

In some applications with high source resistances and low load resistances, this equation could be greatly simplified, but not for cycloconverters. In the cycloconverter, R_L is significantly higher than R_S. These resistances are actually impedances. However, the operating frequency is constant so the impedances are constant resistive values.

The load resistance is calculated by dividing the output RMS voltage (50 V_{PEAK}) by the full load RMS current (10 A_{RMS} full load). The source resistance is not so easily calculated. A rough estimate erroring on the low side is obtained by assuming the high frequency source has no resistance and therefore the only

resistance is introduced by the thyristors. The thyristors resistance is usually found from their forward voltage drop at different load currents using a graph on the datasheet.

$$V_{Out} = \frac{50V_{Peak}}{\sqrt{2}} = 35.4V_{RMS} \tag{3-15}$$

$$\omega_C = 2\pi f_C = 600\pi \tag{3-16}$$

Table 3-5. Filter Calculations

	10% Load	100% Load
V_{Out}	35.4	35.4
I_{Out}	1	10
R_L (Ω)	35.4	3.54
$V_{T\text{-}AnCat\text{-}On}$ (V)	0.9	1.2
R_S (Ω)	1.8	0.24
ω_C (rad)	600π	600π
LC	5.82E-6	4.43E-6

If a value of 400 μF is chosen for C, then L would be 14.6 mH at 10% load and 11.1 mH at full load. These are rough estimates that will be fine tuned in simulation as well as prototyping.

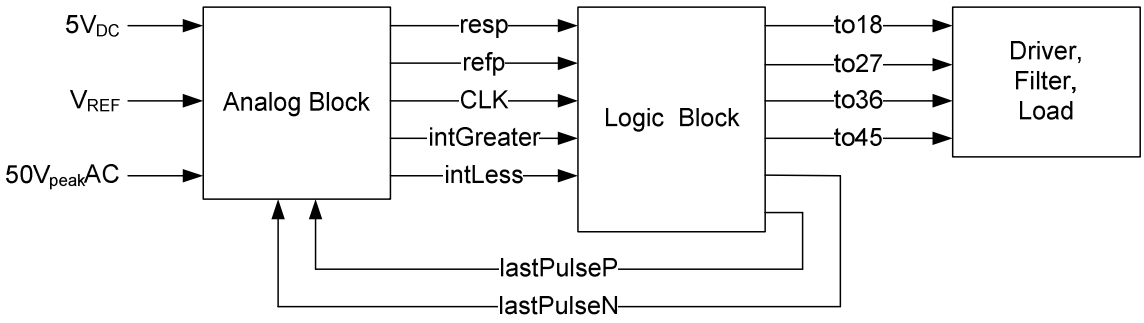

Figure 3-7. Soft Switching Cycloconverter Block and Signal Diagram

The converter has been designed and is now ready for simulation. There are several details that will come into play at different stages of simulation and prototyping involving specific circuitry and design implementation that are neglected here. The basic implementation, however, has been split into fairly concise blocks with connecting signals. The complete layout is organized and fits together as shown in Figure 3-7.

Chapter 4. Simulation and Analysis

4.1. Simulation Methods

From a control standpoint the soft switching cycloconverter described in this thesis can be broken down into three blocks as previously shown in Figure 3-7. The first two blocks are the analog and logic control sections, while the last block combines the rest of the converter. In order to get a better understanding of the control system and to verify the control techniques described in section 3.3, a Simulink model was developed.

After the Simulink model verified and aided in fine tuning the control techniques, the power stage and output filters, the design was ready to proceed to the circuit level. The circuit level design was simulated using OrCad PSpice. This provided a much more accurate simulation because it used PSpice models of the exact components that would be used to implement the hardware design. These included models for specific comparators, op-amps, logic gates, transistors, photocouplers and thyristors. This simulation proved specific techniques that were purely mathematical in the Simulink model, such as the "CLK" generator in Figure 3-5.

4.2. Simulink Simulation

The Simulink simulation diagram is shown in Figure 4-1. The simulation starts with the “Vref” block in the center left hand side, where the 60 Hz reference sine wave is generated. This goes through an amplifier to scale the wave, thereby adjusting the output average pulse density and filtered peak voltage.

The reference is then split and fed into a comparator to determine the “refp” signal, as well as into the integrator summing junction. The integrator summing junction also adds in the feedback signal “lastPulseN” and subtracts the feedback signal “lastPulseP” to form the input to the “discreteIntegrator”. Using these signals the integrator output tracks the build up of discrepancy between the average output and the reference input. This output is monitored by two comparators, one for the high threshold that triggers a high output pulse and one for the low threshold that triggers a low output pulse.

At the top left the input source “AC V Src” is measured and compared by “COMP2” to generate the “resp” signal. The same signal is also full bridge rectified using an absolute value block “FBRect” and compared to the value 45, which is near the 50V peak of the source. This generates the clock signal using the same method previously described and illustrated in Figure 3-5. This concludes the analog block from the block diagram in Figure 3-7.

The analog block signals are measured by the virtual oscilloscope “OS1”. Figure 4-2 is a zoomed view of “OS1” showing “AC-Input”, “CLK” and “resp”. Figure 4-3 shows “OS1” over a full period of the output waveform to show “refp”, the compared integrator outputs and the feedback signals.

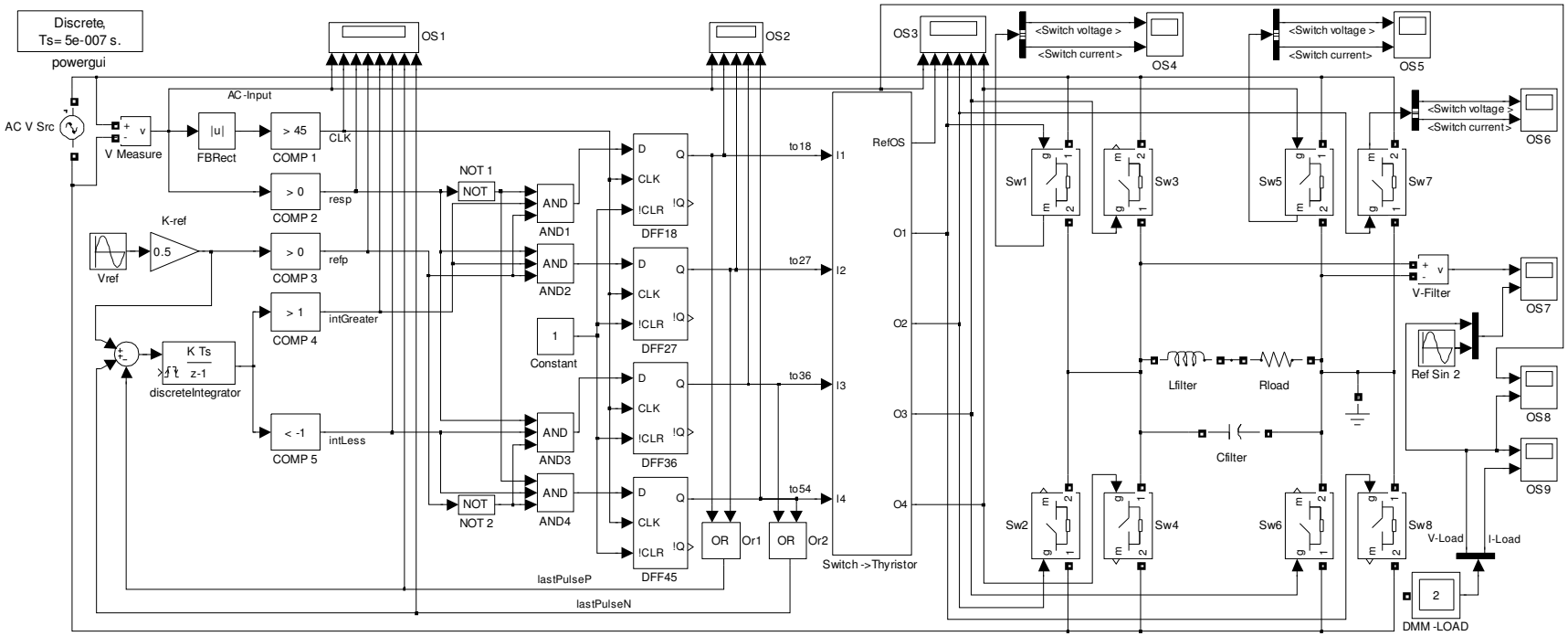

Figure 4-1. Simulink Model

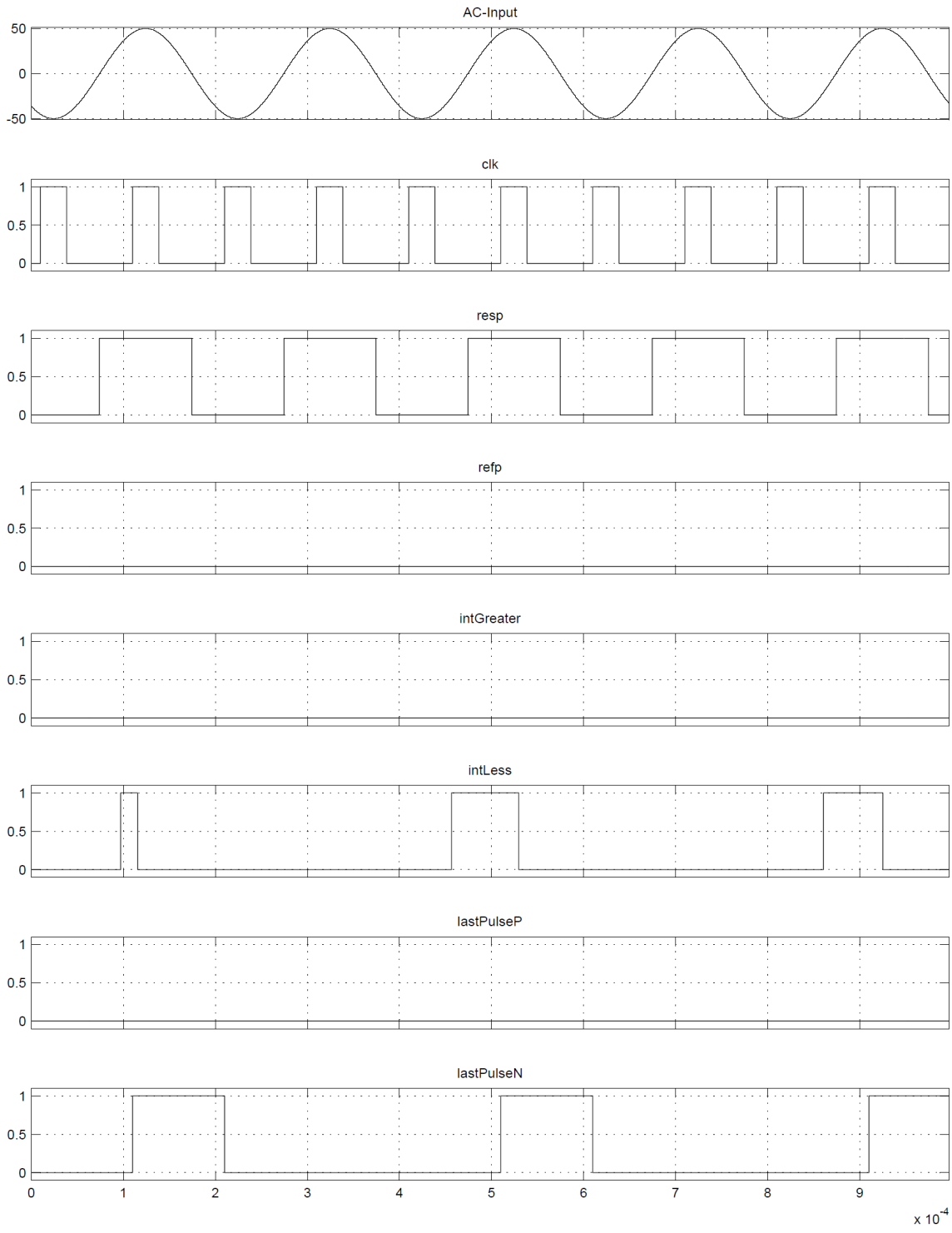

Figure 4-2. Simulink “OS1” Analog Control Waveforms Up Close

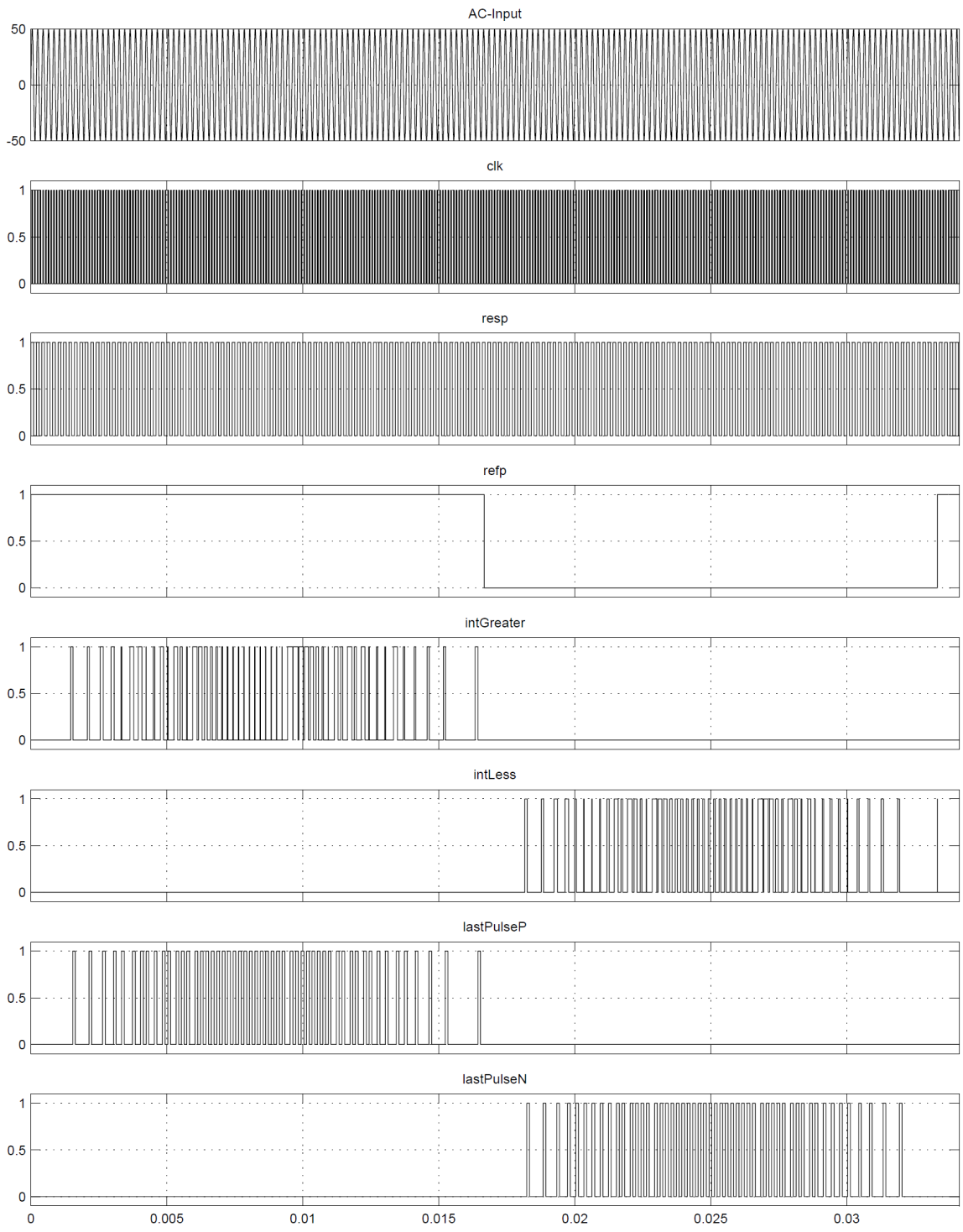

Figure 4-3. Simulink “OS1” Analog Control Waveforms One Period

The signals now enter the logic block. In this block they are combined using the “NOT” and the “AND” operators as described by equations 3-4 through 3-7. After this the signals are fed into D flip flops and outputted to the drivers. This concludes the logic block. The signals going to the drivers are shown in Figure 4-4. The driver signals “to18” and “to27” represent the positive half cycle of the output waveform. Adding (logical OR) these two waveforms together produces “lastPulseP” from Figure 4-3. Likewise, “to36” and “to54” added together produce “lastPulseN”.

The next block in the Simulink model is named “Switch->Thyristor”. This is a subsystem consisting of four D flip flops and a clock signal which, for proper operation, must be set to twice the frequency of the “AC V Src”. This block makes up for a deficiency in Simulinks switch models. This subsystem and its output lines are not present in the physical design. The issue is that Simulink switch models don’t behave like PSpice switch models. Their gates are not modeled from a circuit standpoint, with voltages and currents, but rather from a digital control standpoint with either a high or low (on or off) value.

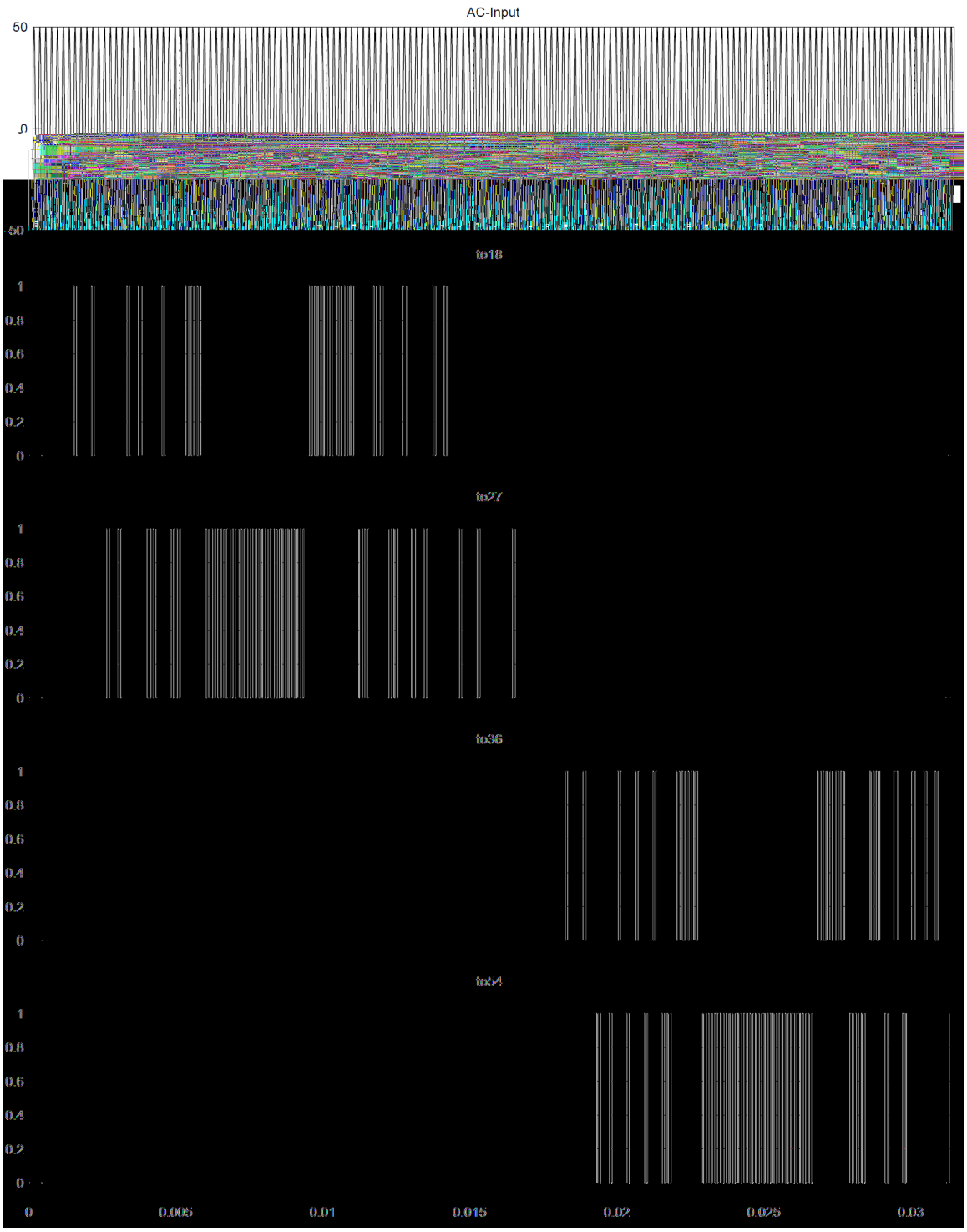

Figure 4-4. Simulink “OS2” Logic Block to Driver Waveforms

There are several switches in the Simulink Power Library (“powerlib”). However, they all seem to simply be a resistor if their gate is high and an open circuit if their gate is low. The only difference between these switches is the addition of parallel diodes and snubber circuitry. They are all essentially bidirectional fully controllable switches. To account for this, the “Switch->Thyristor” block adjusts the gate signals so the thyristor is only on when forward biased.

The thyristor driver block is not incorporated into the Simulink model because, as previously mentioned, the switch used is controlled by Simulink signals and not gated at the circuit level using voltage and current as in traditional circuit analysis software. The eight thyristors are labeled in the simulink model as “Sw1” through “Sw8”. They are shown out in Figure 3-2 with the filtered load configured as seen in Figure 3-6. The switch voltage drop and current are observed by scopes “OS4”, “OS5” and “OS6”. However, these don’t contain clearly decipherable trajectories and, therefore, were not included in this thesis.

The unfiltered output from scope “OS7” is seen in Figure 4-5. This waveform shows the monopolar pulse density modulation of 50V-peak pulses. It is noted that these pulses, or half cycles of the high frequency input, are staggered so their density varies sinusoidally. To convert this to a clean sinusoid, however, the high frequency components must be filtered out.

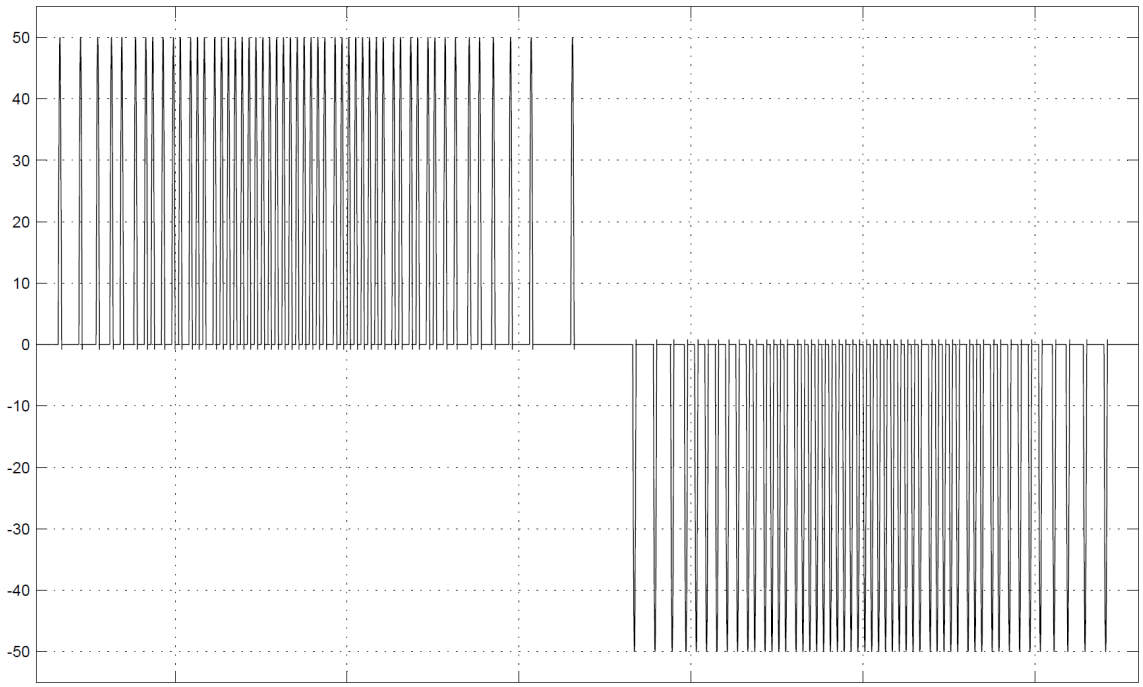

Figure 4-5. Simulink Unfiltered Output “OS7” with R = 3.5 Ω

The input and output voltage zero crossing transition is shown in Figure 4-6 for both the converter input and referenced output. Notice how some positive pulses in “V-Load” come from positive pulses in “AC-Input”, while other positive pulses in “V-Load” come from negative pulses in “AC-Input” and likewise with negative pulses in “V-Load”.

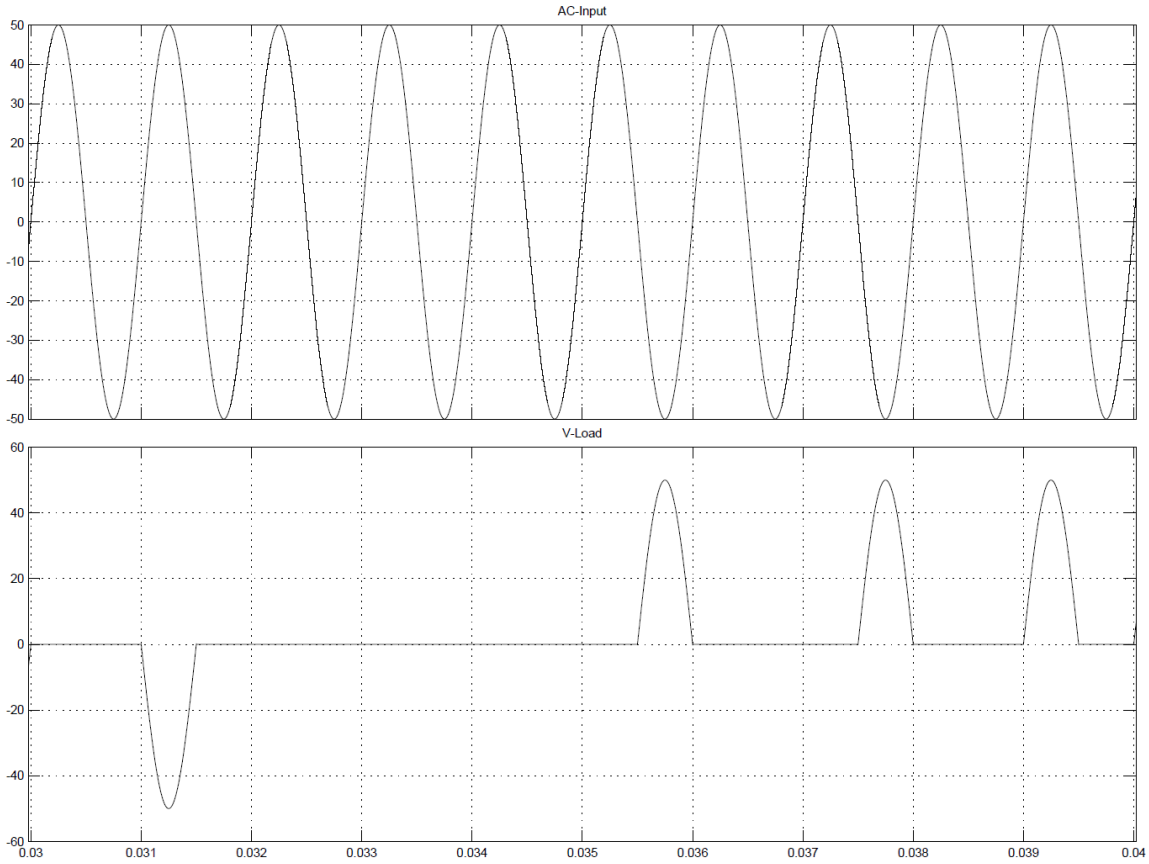

Figure 4-6. AC Input and Output Voltage Zero Crossing Transitions

With the filter set to the parameters from the example after Table 3-5, the filtered output is not completely sinusoidal. There are several kinks, as shown in Figure 4-7. This is due to the capacitor being too small and unable to supply the inductor with enough current when the thyristors are off. To compensate for this, the capacitor was increased by a factor of three, while the inductor was decreased by a factor of three. The effect, as seen in Figure 4-8, is less distortion, but more ripple due to a smaller inductor. The waveform is also slightly higher in amplitude.

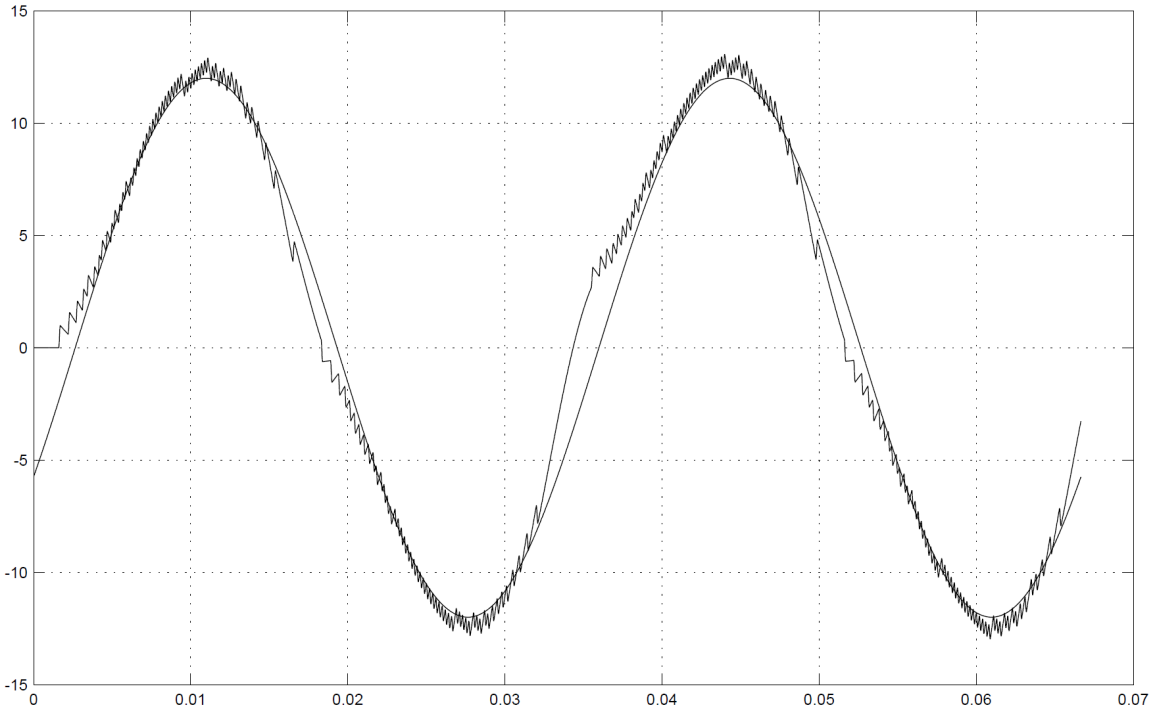

Figure 4-7. Simulink Filtered Output with L = 11.1 mH, C = 400 μF and R = 3.5 Ω

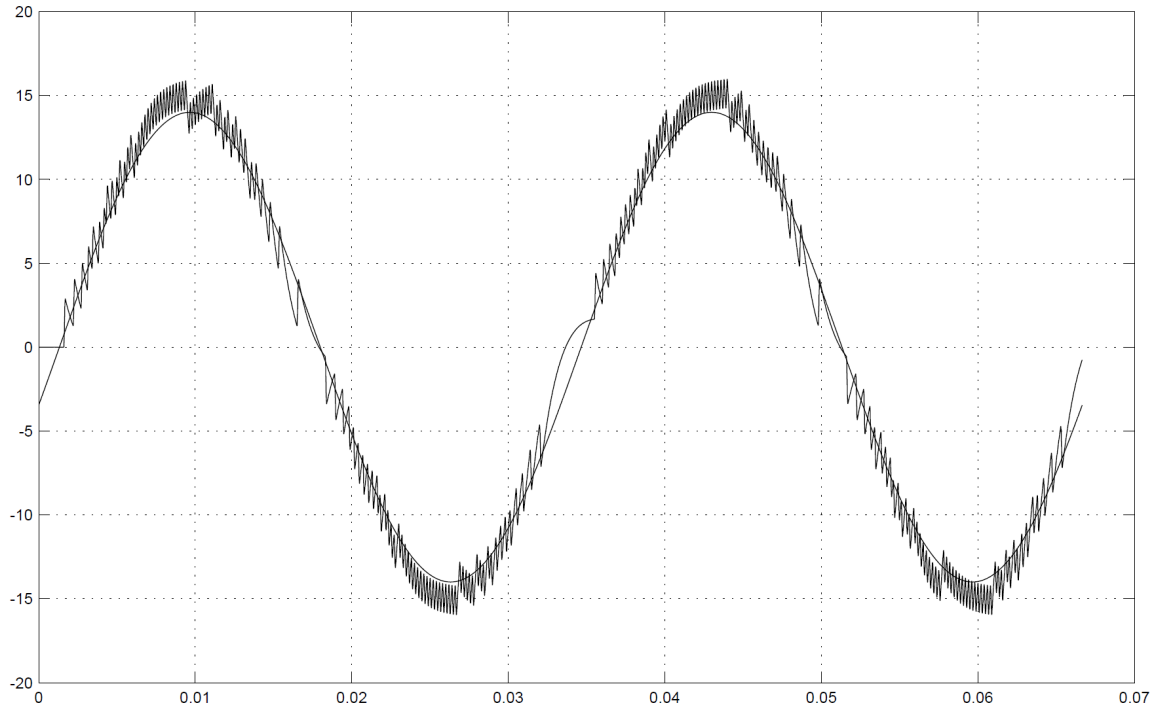

Figure 4-8. Simulink Filtered Output with L = 3.7 mH, C = 1200 μF and R = 3.5 Ω

Both filtered waveforms above are fairly rough looking. Smoothing them out requires increasing both the inductor and capacitor, which will in turn lower the cutoff frequency of this low pass filter. This was explored by roughly doubling the calculated values for each component in Table 3-5, resulting in the output waveform in Figure 4-9. This larger filter produces a significantly smoother waveform; however, it cuts into the fundamental amplitude, reducing it by almost one third.

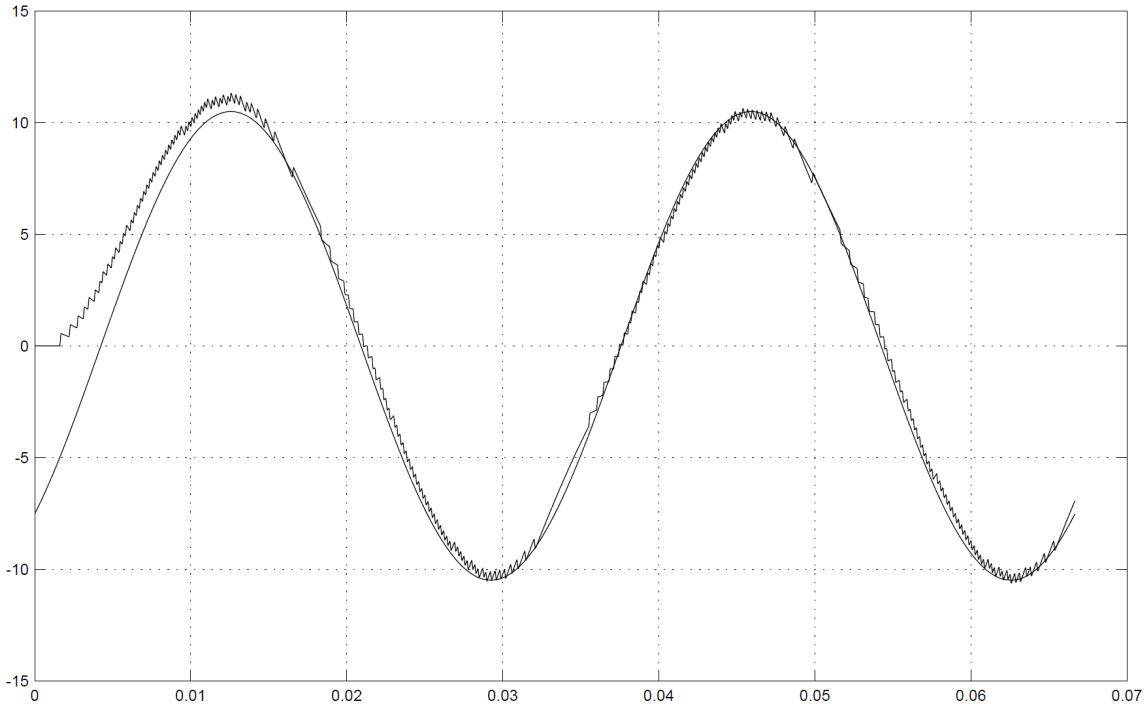

Figure 4-9. Simulink Filtered Output with L = 20 mH, C = 2000 μF and R = 3.5 Ω

4.3. OrCad Simulation

Though the Simulink model showed that the soft switching cycloconverter could work mathematically, it was still a fair leap to get to a functional circuit. Many of the Simulink blocks were not in the form of standard circuit components. This included the integrator, the comparators and the thyristor driver circuitry. In order to fine tune the model and develop the specific circuit component layout, OrCad PSpice was used.

OrCad was avoided for the initial simulation because it is less suitable to complex control circuitry, especially when using integrated circuits (ICs) like microcontrollers and field programmable gate arrays (FPGAs) that have user defined properties. Once the control circuitry was mapped out in Simulink, it was realized that the controls consisted only of an integrator, some comparators, a few logic gates and some flipflops. This was easily simulated in OrCad using specific component models for most of the specific chips purchased to implement the design.

The first stage of the OrCad model is the Analog Block starting in Figure 4-10. This figure shows the reference signal as well as the integrator with feedback. There are several resistors that are shown as variable. These will be implemented in the final design as potentiometers to allow exact calibration of resistor ratios.

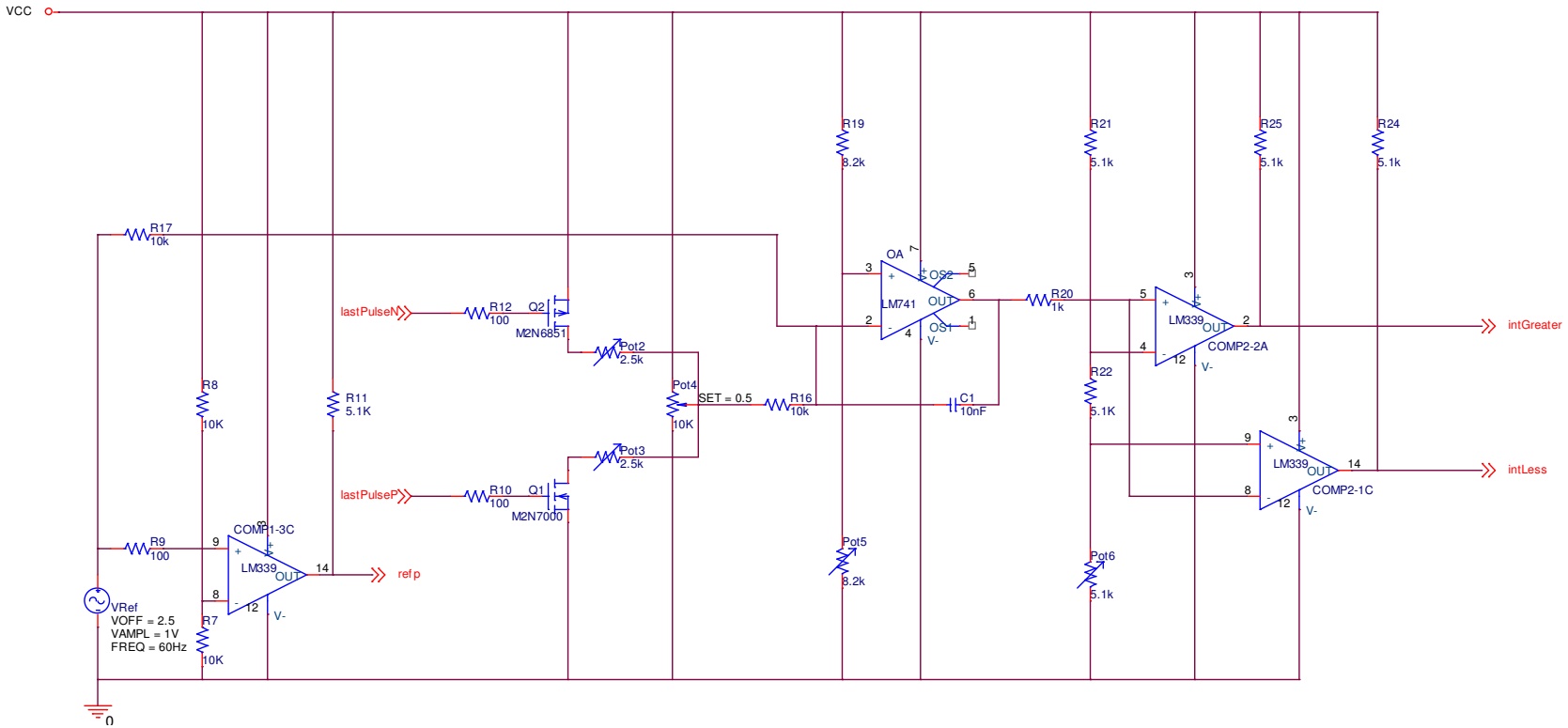

Figure 4-10. OrCad Analog Block

The integrator is set to integrate up and down with its origin at 2.5 V. This is set by the op-amp “OA” non-inverting input pin 3. This pin is set to 2.5 V by making “Pot5” equal to “R19”. The amplitude of the cycloconverter output is adjusted by changing the ratio of the feedback signal amplitude to the reference signal amplitude. This is accomplished by simultaneously adjusting “Pot2” and “Pot3”, or adjusting the reference amplitude. “Pot4” must be set as close to its center as possible so that when there is no feedback (“Q1” and “Q2” are off) there will be no current through “R16” into the integrator.

The Analog Block is continued in Figure 4-11. This shows the clock generation derived from Figure 3-5. “Pot1” adjusts the voltage to “COMP1-1” so its maximum at the peak of “Vsrc” remains under the 5 V rails.

Figure 4-12 contains all the inputs from the Analog Block, as well as the driver and feedback outputs. The driver outputs transition to Figure 4-13 where they control the thyristors via the photocouplers “PHOTO1A” through “PHOTO4B”. This is done according to Figure 3-3 with a slight modification. Because the BJT’s in the photocouplers chosen for the design had a 30 V forward breakdown and a 6 V reverse breakdown, zener diodes “D15” through “D22” were added. These short the BJT’s reverse voltage to the diode forward voltage drop of around 1.2 V and clamp the BJT’s forward voltage to the zener voltage. The zener voltage is set to 10 V for this simulation, but will be 12 V for the hardware and could be anywhere below 30 V. A zener voltage closer to 30 V would limit zener losses; however, due to current availability 12 V will be used.

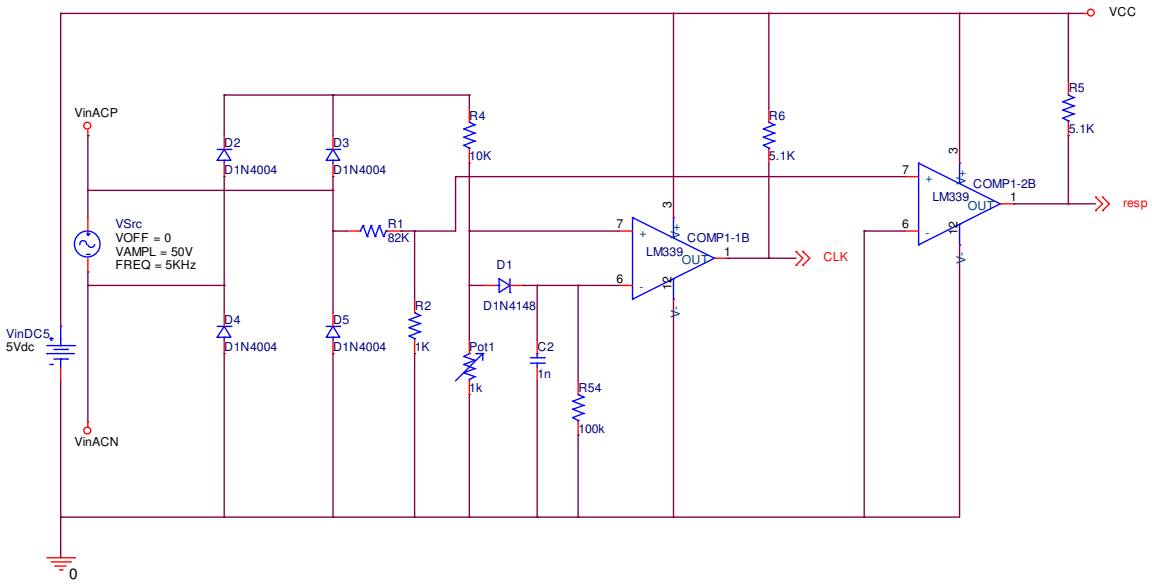

Figure 4-11. OrCad Analog Block Continued

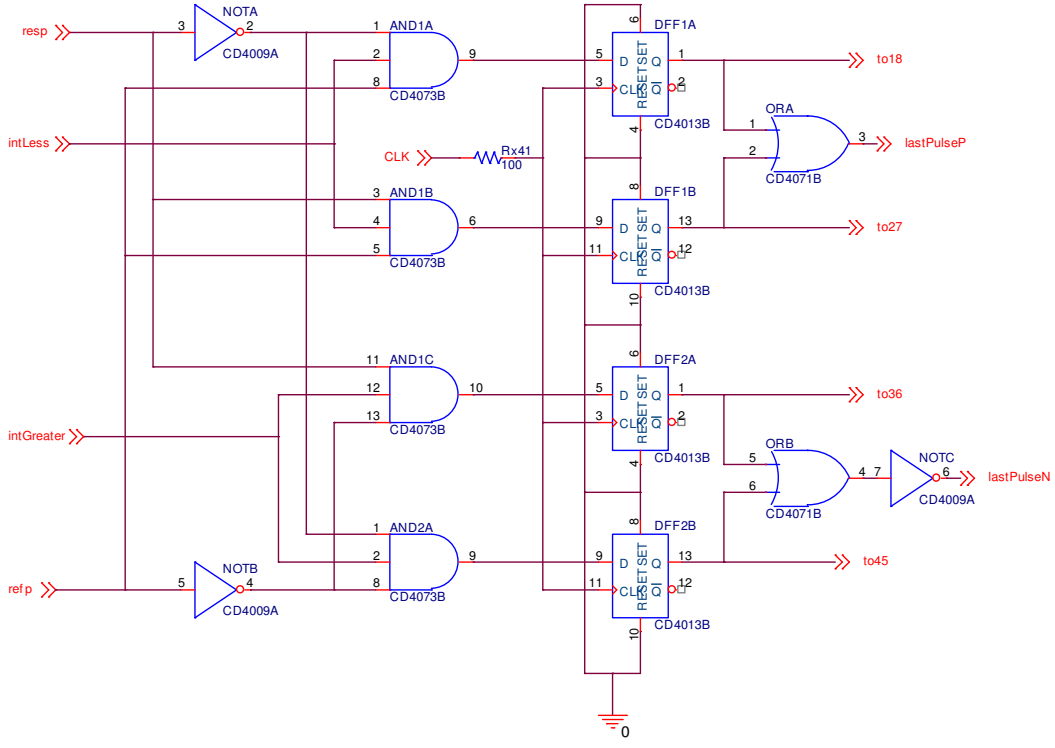

Figure 4-12. OrCad Logic Block

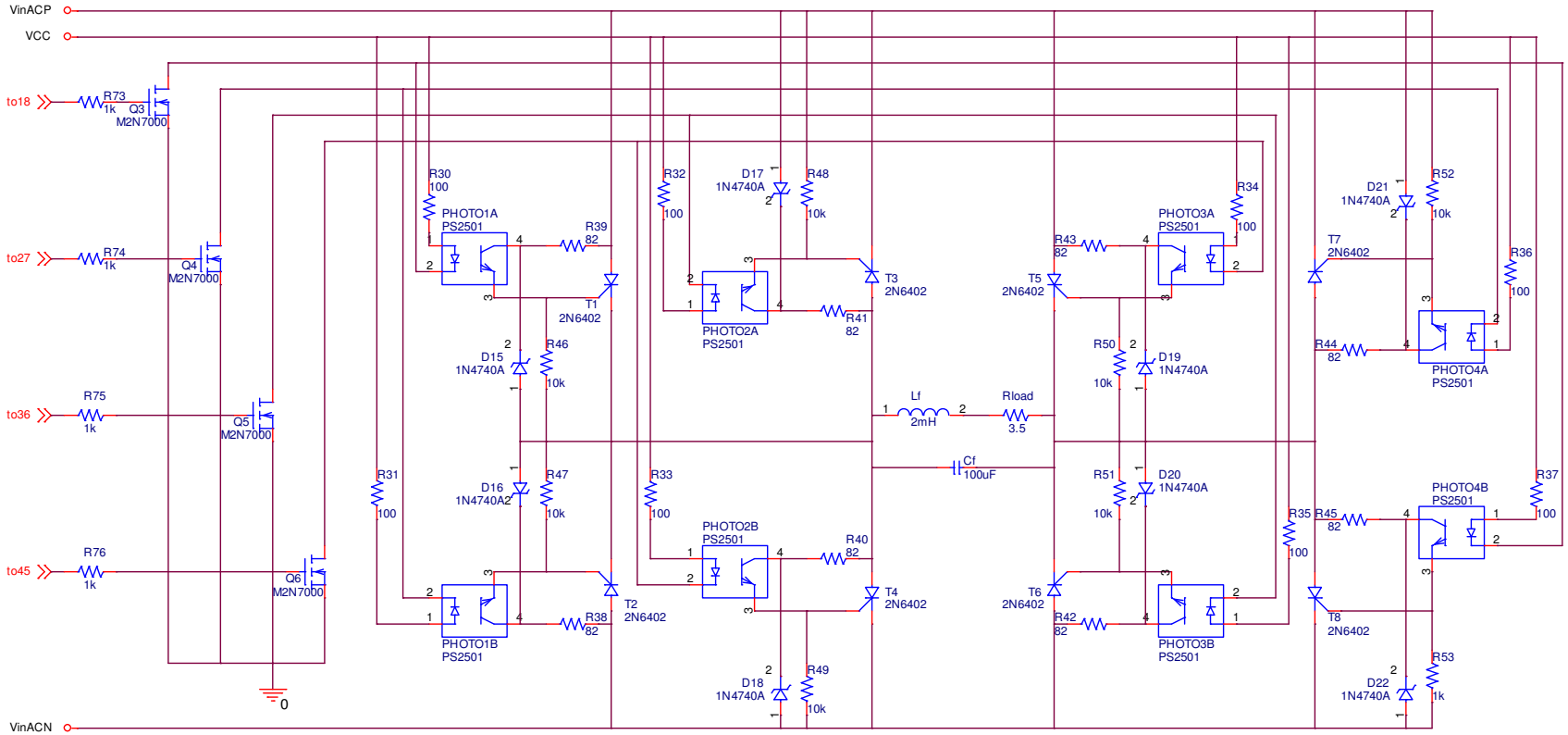

Figure 4-13. OrCad Power Stage

The OrCad simulation had a lot of convergence problems. To understand convergence problems, it is important to understand PSpice. PSpice writes equations relating voltages and currents at and between each node and then solves them simultaneously. There are so many equations that the only way to solve them is iteratively, using some form of the Least Squares Method. This is done by guessing initial values for each current and voltage, feeding these into the equations, solving them for new currents and voltages, feeding these into the equations and repeating until the outputs converge within a specified tolerance.

Iterative solving has three weaknesses. First, the initial guess has to be close enough to start convergence towards the correct value. Second, the functions must be continuous enough that as the solver “walks” in one direction it can tell if it is getting closer or further to convergence. Finally, if the function converges, there is always the possibility that it converged on some local minimum that was not the best answer in the entire answer plane.

To help PSpice converge, it is important to have a path to the ground and power rails through pure resistors from each node in the circuit. This is shown in Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18 as every resistor with an “x” in its designator. Also added in Figure 4-17 are capacitors “Cx1” and “Cx2”. These are used to avoid the “hazard” produced when the OR gates “ORA” and “ORB” experience both their inputs changing at the same time. These capacitors along with “Rx7” and “Rx9” delay the transition of one of these inputs, allowing the simulation to run with fewer errors. In the actual hardware implementation, the hazards are not important because a tiny output blip on the OR gates will

translate into a tiny error in the integrator. This will only have a slight and insignificant effect on THD for a given half cycle.

Another convergence aiding technique used in this simulation was increasing the convergence tolerances in the simulation profile options menu. Both the voltage and current accuracy were greatly increased as seen in Figure 4-14 below.

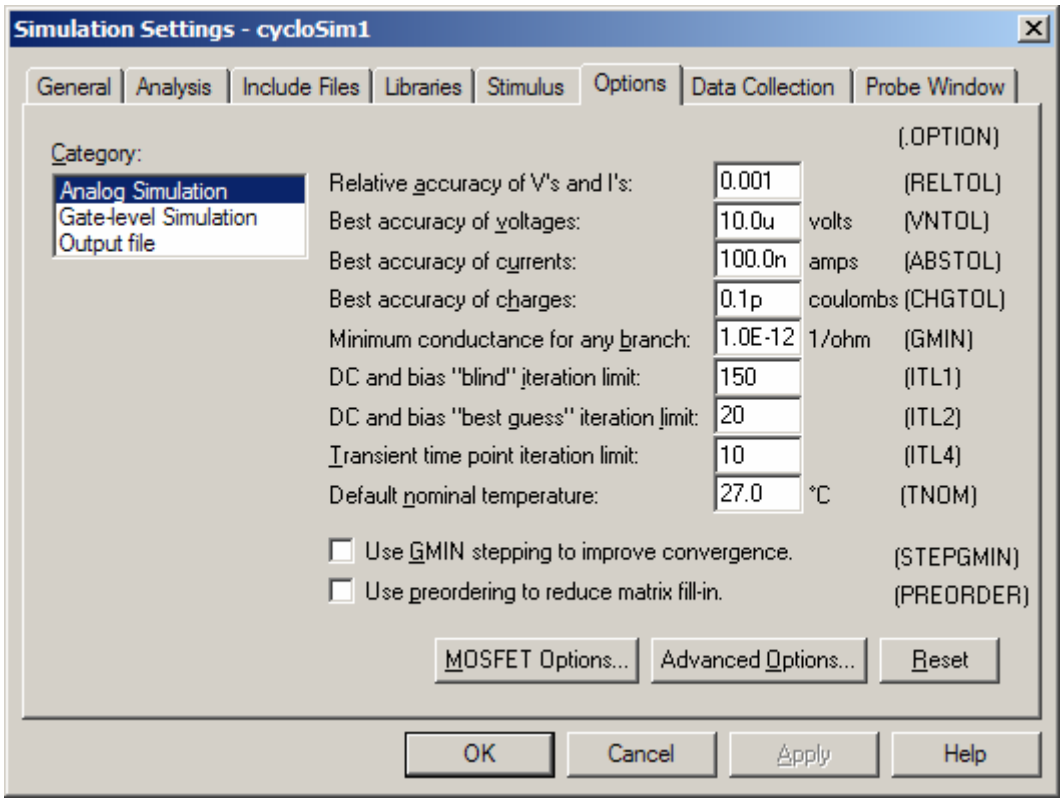

Figure 4-14. OrCad Simulation Convergence Tolerances

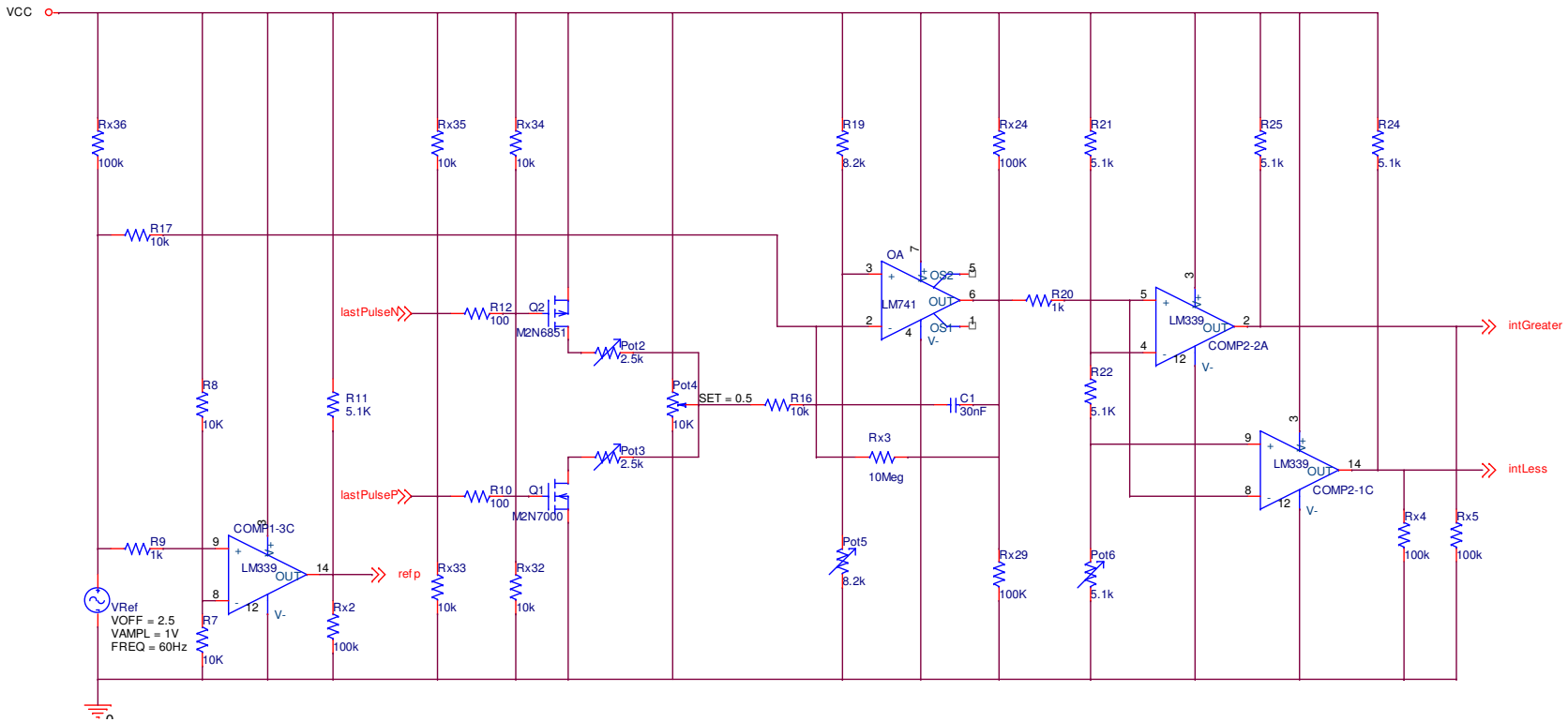

Figure 4-15. OrCad Analog Block with Simulation Extras

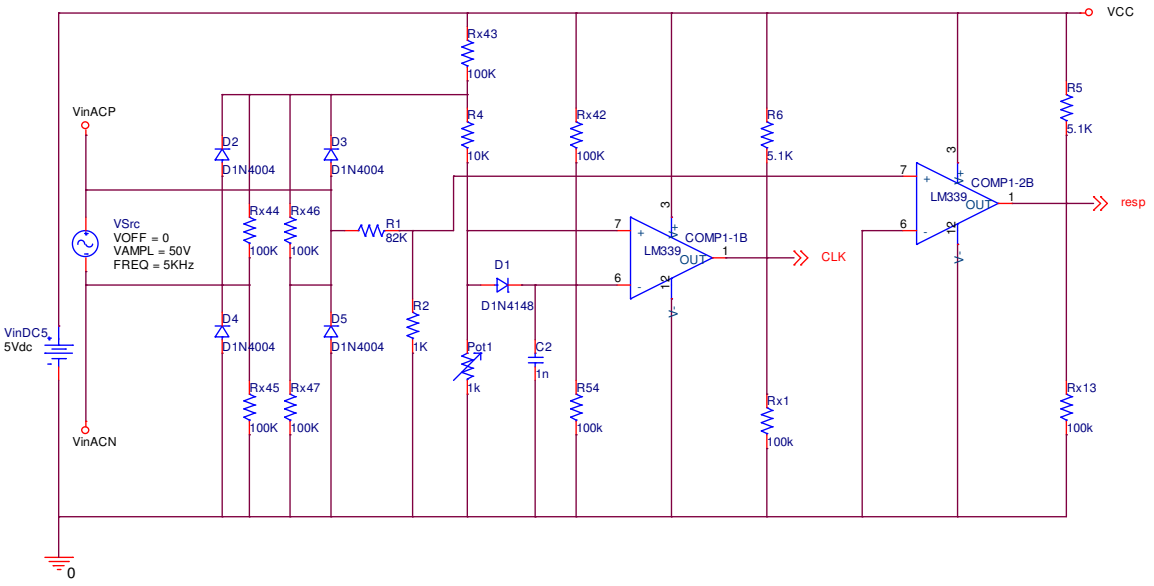

Figure 4-16. OrCad Analog Block with Simulation Extras Continued

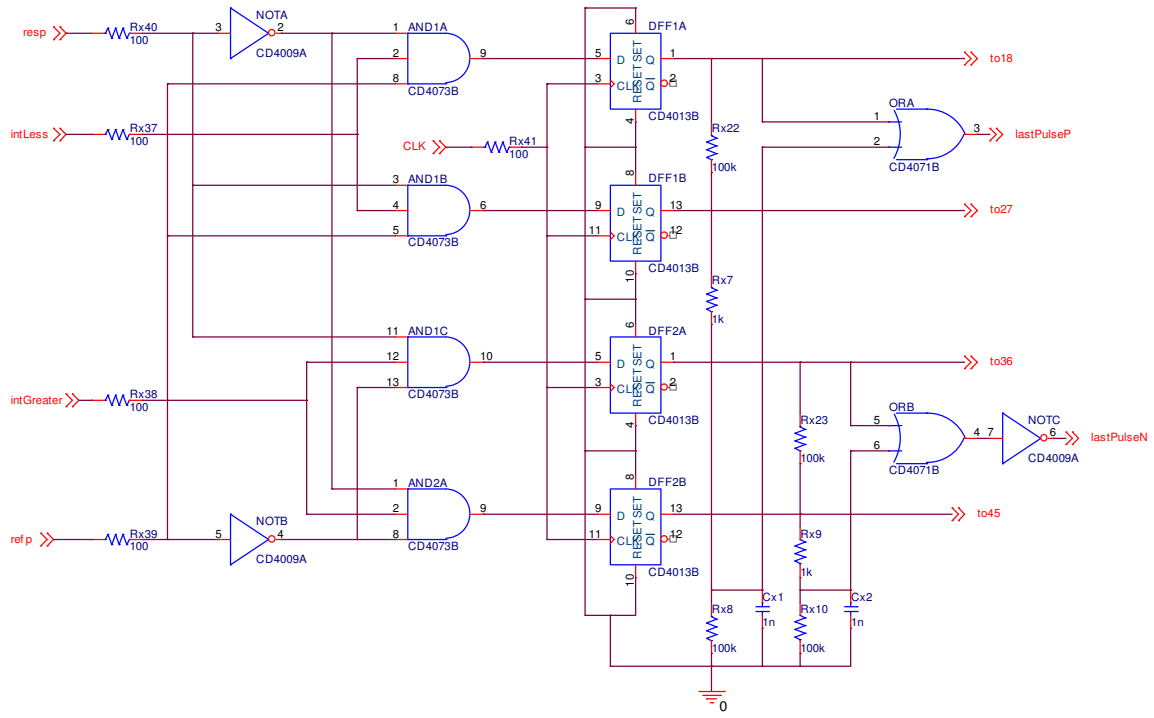

Figure 4-17. OrCad Logic Block with Simulation Extras

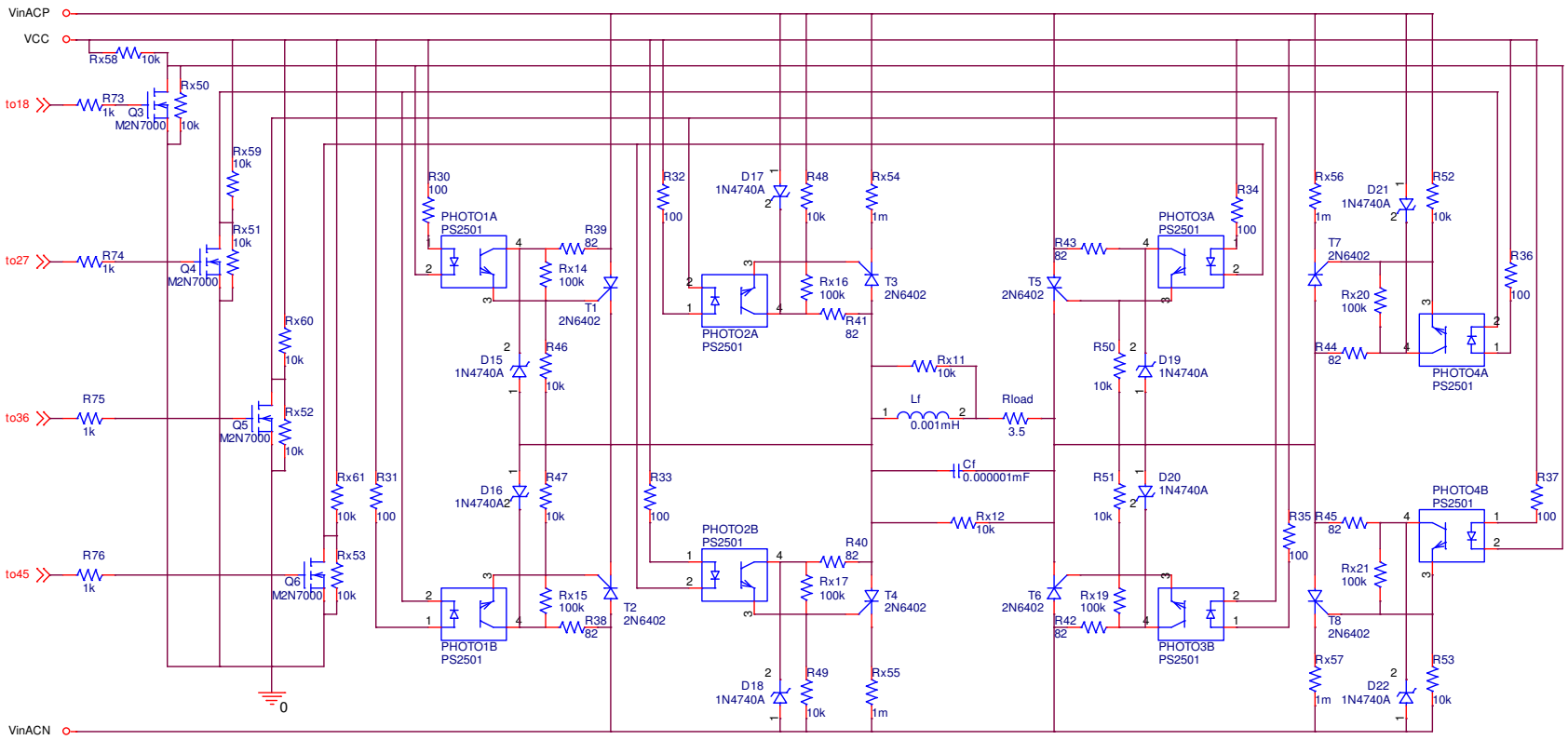

Figure 4-18. OrCad Power Stage with Simulation Extras

Using the modified simulation with extra resistors and capacitors, the voltage across the integrator capacitor (positive referenced at output) is shown in Figure 4-19. The capacitor “C2” in Figure 4-16 was increased to 30 nF to aid in viewing the integrator rise and fall.

As “VRef” falls past the 2.5 V origin, it begins to sink current from “C1” through “R17”. The op-amp “OA” then raises its output voltage to keep its inputs equal, charging “C1”. This continues until the 3.3V threshold of “COMP2-2” is reached, triggering “intGreater” high. This causes the Logic Block (Figure 4-17) to trigger a negative output pulse using “to36” or “to45”. This pulse is fed back through “lastPulseN” to “Q1”, which lowers the output of “OA” by sourcing current to “C1” through “Pot2”, “Pot4” and “R16”. In this case “intGreater” and “intLess” are swapped in the logic block to account for the inverting integrator.

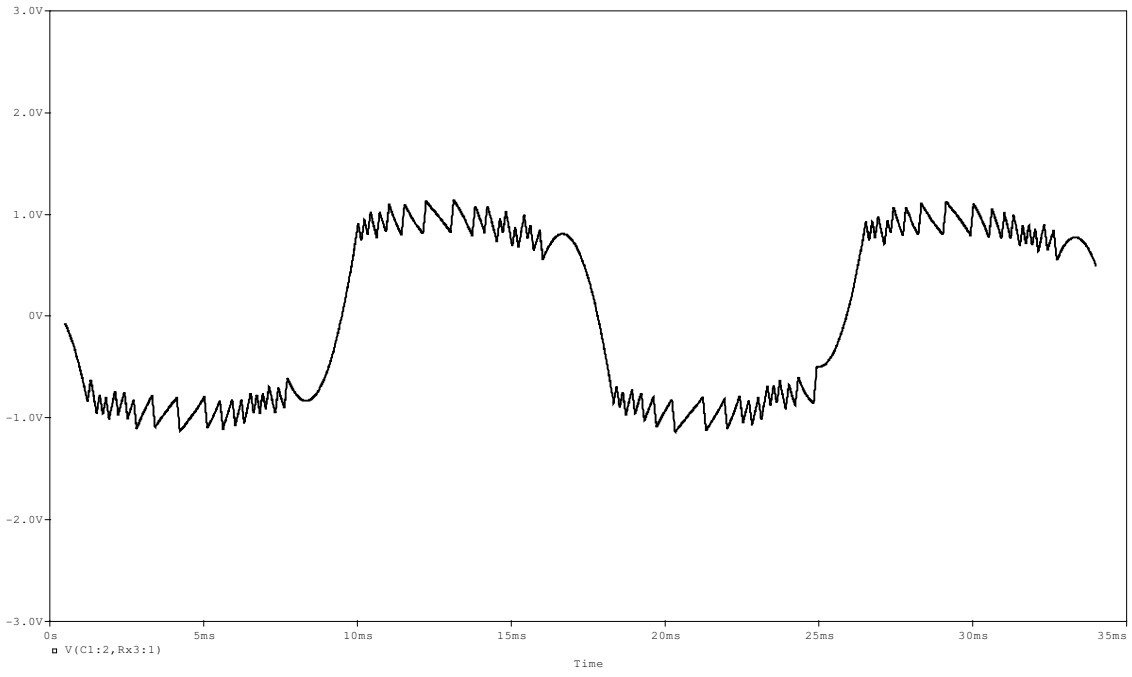

Figure 4-19. OrCad Integrator Voltage with C2 = 30 nF

The output waveform without filtering is shown in Figure 4-20. This shows each pulse peaking around 50 V and pulse density modulated to the 60 Hz reference sine wave. The THD is very high, as expected, which is further detailed in the waveform FFT Figure 4-21.

Figure 4-22 and Figure 4-23 show the filtered output with filter values from the Simulink model in Figure 4-8. Likewise, Figure 4-24 and Figure 4-25 show the filtered output with values from the Simulink model in Figure 4-9. In both cases, the waveform produced by the OrCad model shows significantly more distortion than the Simulink model.

The additional distortion may derive from a combination of differences between the OrCad and Simulink models. The first difference is the integrator. The integrator thresholds are not equivalent. Their ratios of reference to feedback gain differ and they have different integration rates. Also, converter output resistance to the filter is likely significantly different, requiring a different CL filter.

Figure 4-26 and Figure 4-27 show a cleaner waveform using a larger filter. These values, especially the capacitor, are fairly large relative to available components. The hardware design will have to utilize a smaller filter due to budget and practicality constraints. Besides this, the capacitor is unreasonably large in this filter, passing significant 60 Hz current and severely degrading converter efficiency.

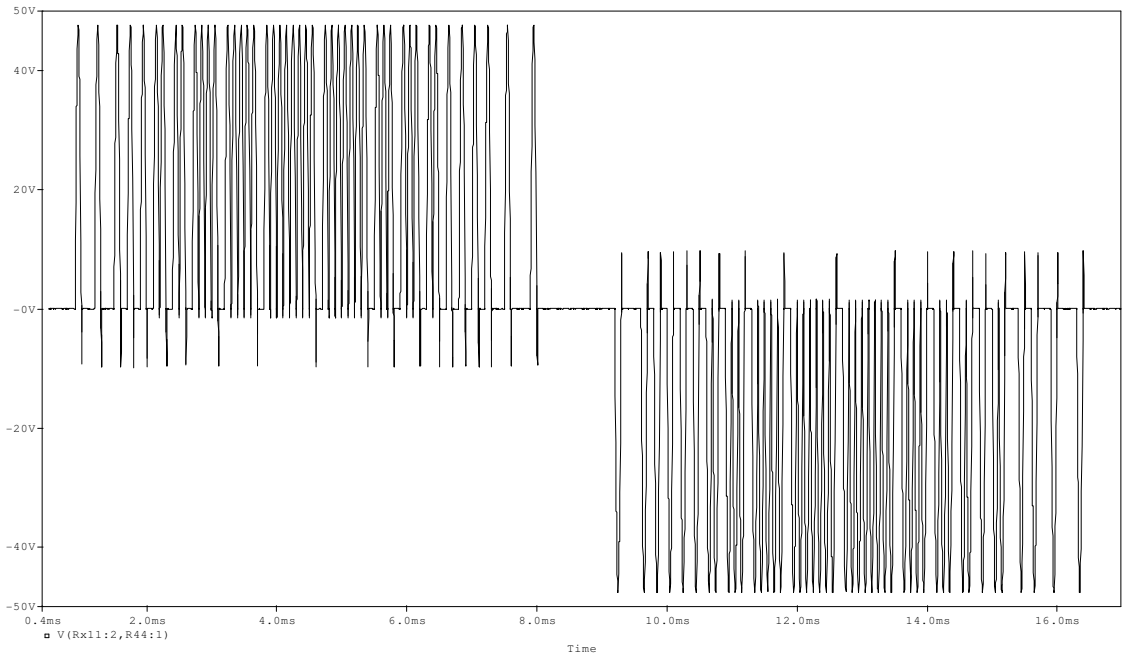

Figure 4-20. OrCad V_{OUT} Unfiltered THD = 88%

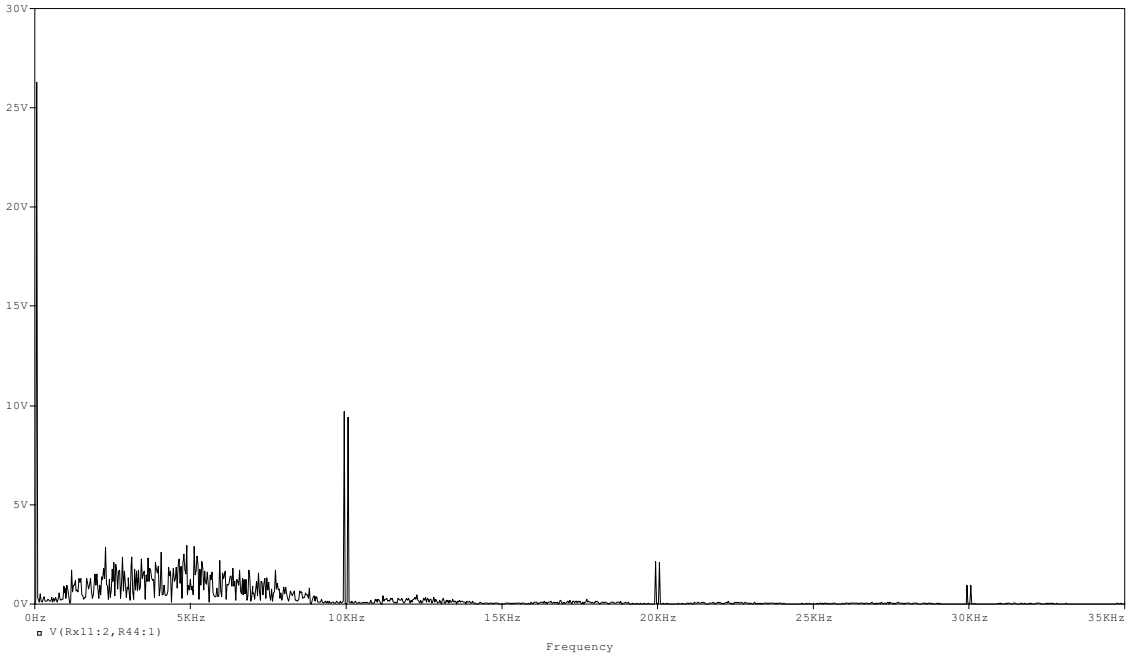

Figure 4-21. OrCad V_{OUT} Unfiltered FFT

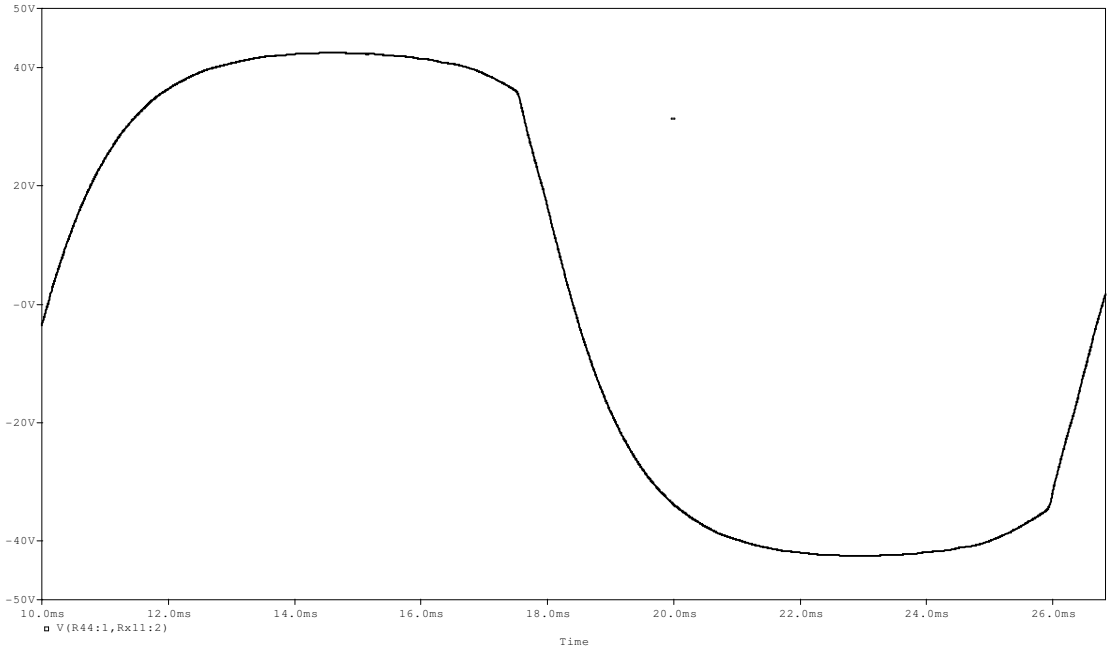

Figure 4-22. OrCad V_{OUT} Filtered L = 3.7 mH, C = 1.2 mF, R = 3.5 Ω, THD = 21%

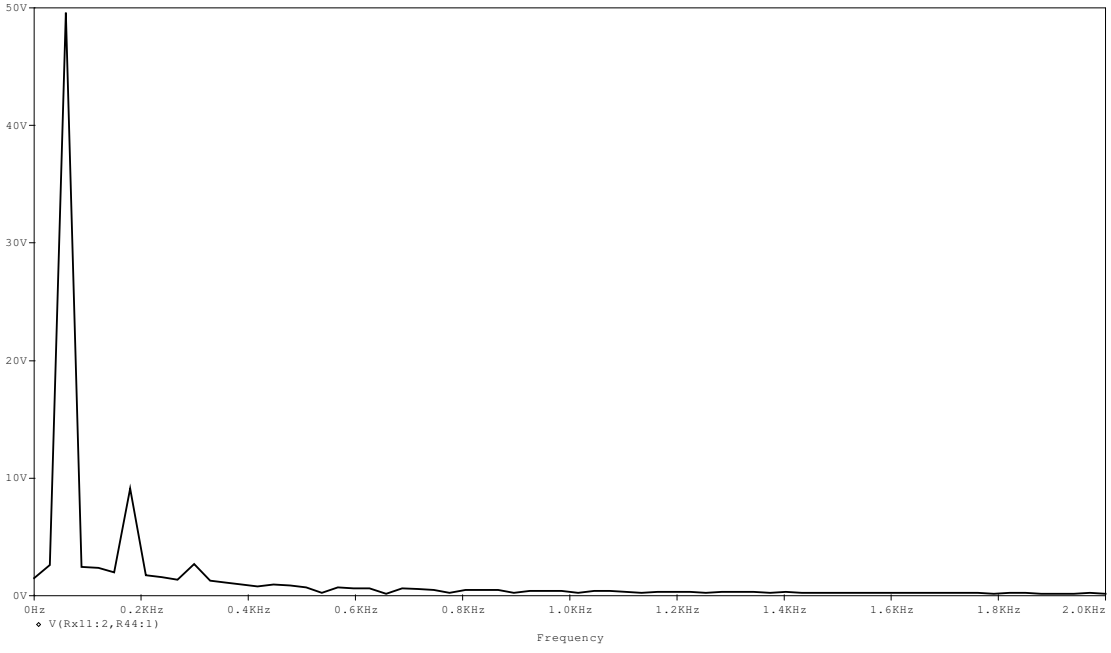

Figure 4-23. OrCad V_{OUT} Filtered FFT L = 3.7 mH, C = 1.2 mF, R = 3.5 Ω

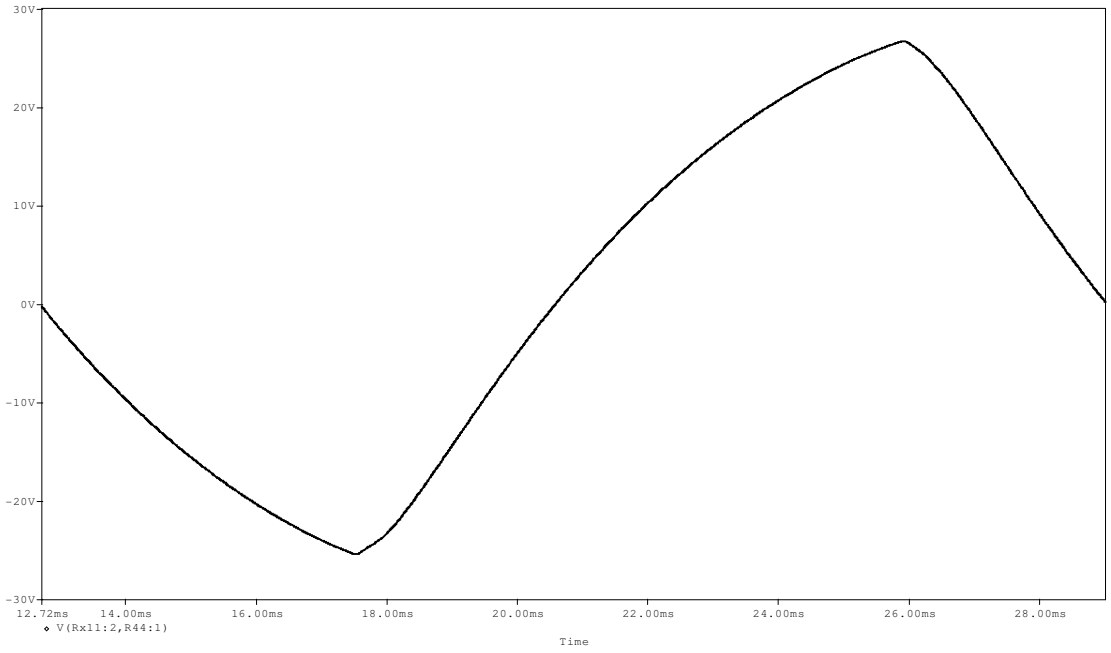

Figure 4-24. OrCad V_{OUT} Filtered L = 20 mH, C = 2 mF, R = 3.5 Ω, THD = 9.9%

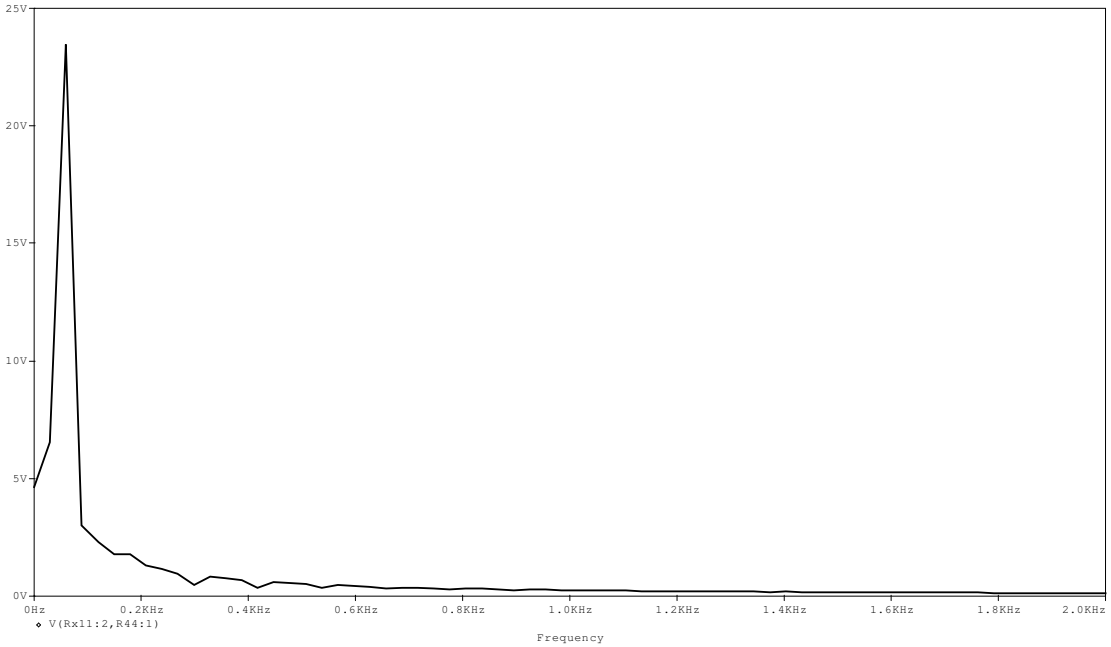

Figure 4-25. OrCad V_{OUT} Filtered FFT L = 20 mH, C = 2 mF, R = 3.5 Ω

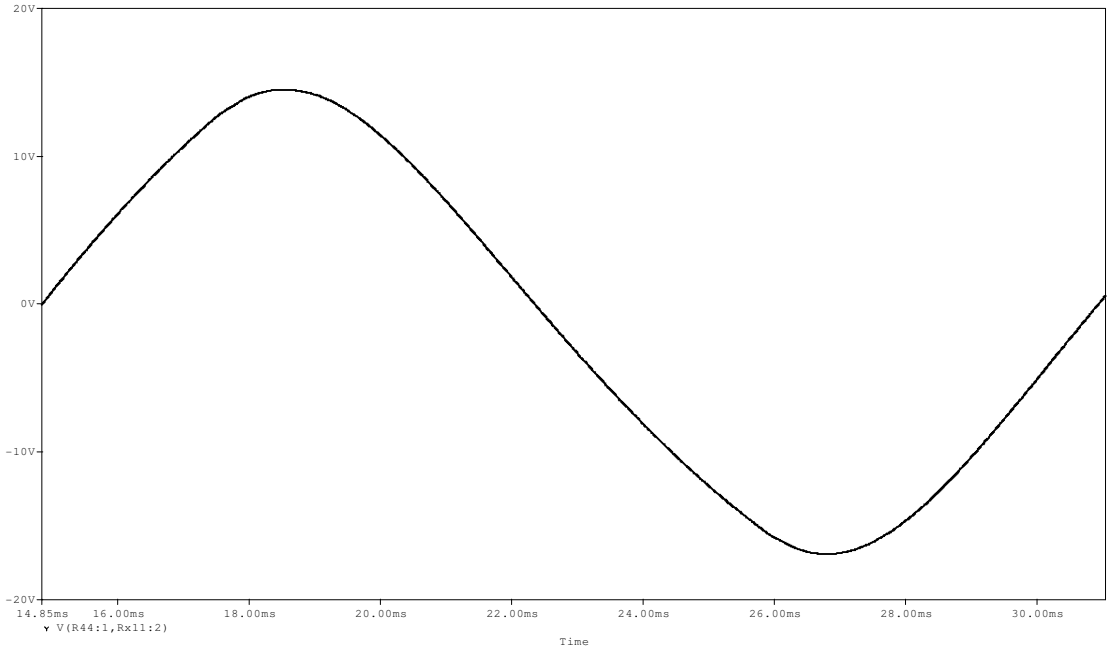

Figure 4-26. OrCad V_{OUT} Filtered L = 20 mH, C = 20 mF, R = 3.5 Ω, THD = 4.5%

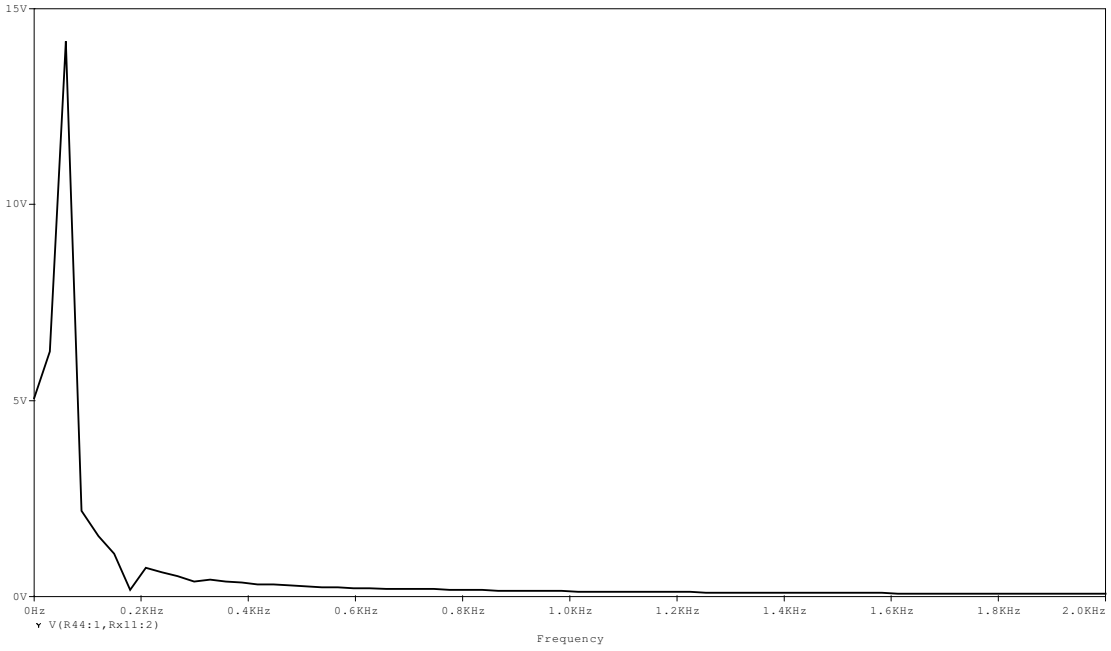

Figure 4-27. OrCad V_{OUT} Filtered FFT L = 20 mH, C = 20 mF, R = 3.5 Ω

The input and output voltage with no filter are compared in Figure 4-28. From this, it appears that the soft turn on is well executed; however there is a spike at turn off that indicates significant thyristor reverse recovery time. This is a property of the thyristor that would be accentuated with increased frequency. Depending on the availability of faster turn-off thyristors, reverse blocking IGBT's may be required when looking into higher frequency designs.

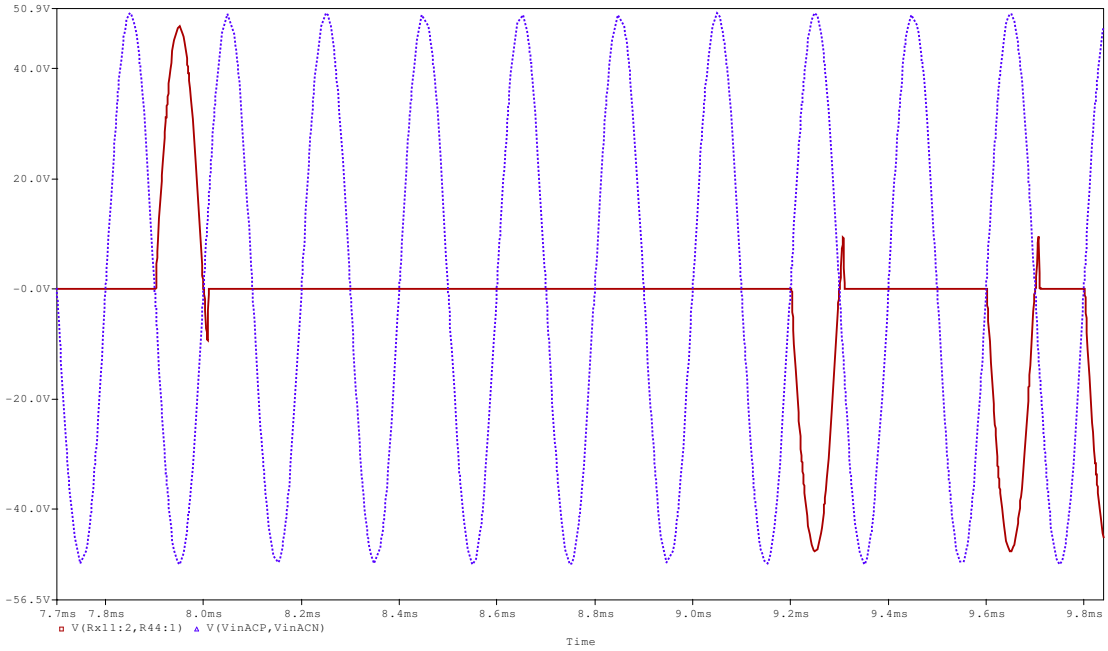

Figure 4-28. OrCad Input and Unfiltered Output (solid is Vload, dashed is Vin)

The voltage and current switching trajectory is shown in Figure 4-29. This shows the zero voltage and zero current soft turn-on. At turn-off, however, the reverse recovery time of the thyristor causes a rougher transition.

The current in this figure is unreasonably large. Once again, this is because the 20mF capacitor used for the filter is passing significant current at 60Hz. The current will be much less in the actual design. However, for the simulation a large capacitor was required to achieve a smooth wave with low THD. The filtered output was shown because it gives the most switching trajectory stress and therefore offers the greatest proof of soft switching.

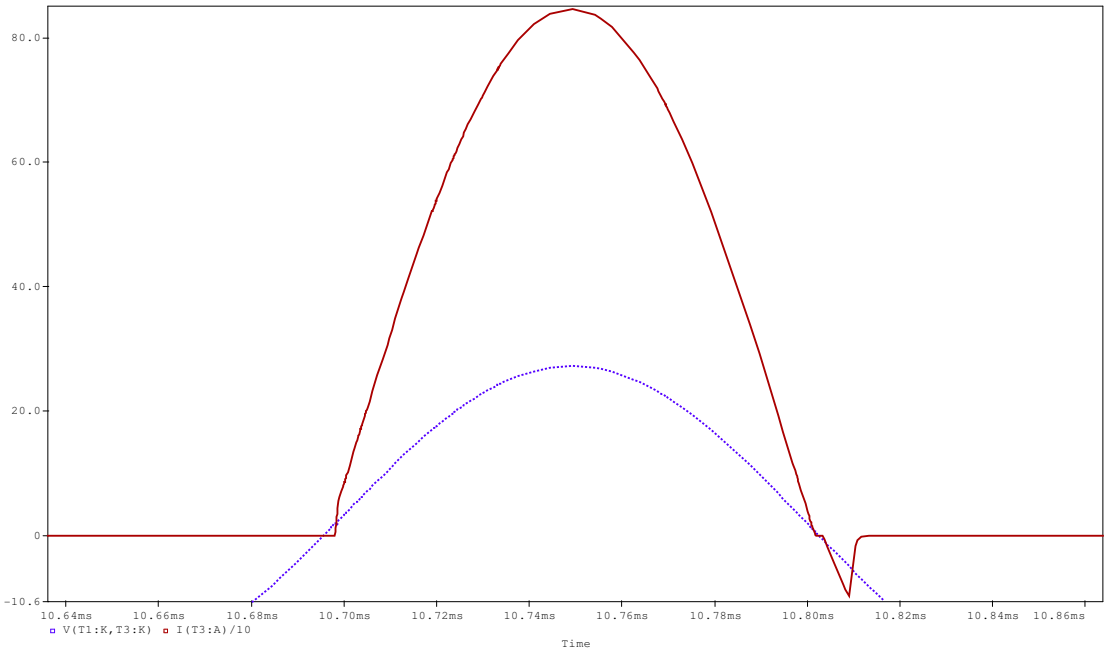

Figure 4-29. OrCad Filtered Switching Trajectory (dashed is V, solid is I / 10)

In this chapter, two full simulations of the soft switching cycloconverter have been performed. First a system level and second a hardware level design have been demonstrated. From here, the designs will be transferred into actual hardware and tested. The test results will be compared with the simulations.

Chapter 5. Hardware Results

5.1. PCB Design

After simulation, the design was transferred to PCB Artist layout software for prototype. The final board was double layer with dimensions 5” x 9”. The layout is seen in Figure 5-1, Figure 5-2, Figure 5-3 and Figure 5-4.

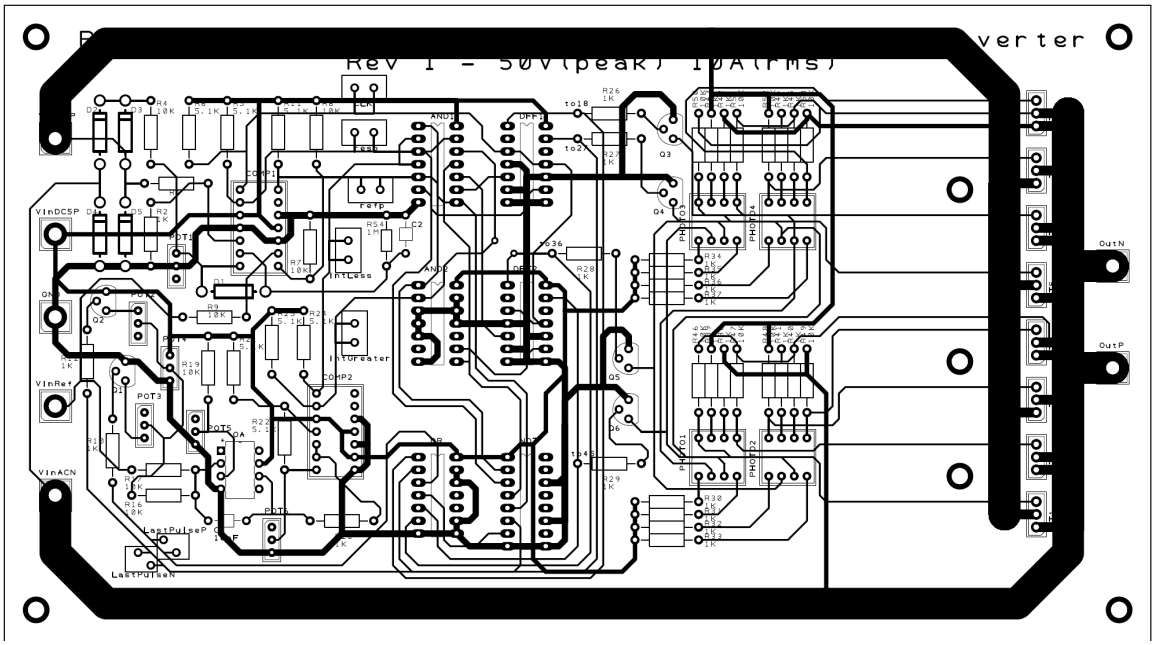

Figure 5-1. PCB Layout: Silk Screen and All Traces

The silkscreen shows component outlines and designators, referenced to the OrCad simulation schematics in Figure 4-10, Figure 4-11, Figure 4-12 and Figure 4-13. It also shows all resistor and capacitor values.

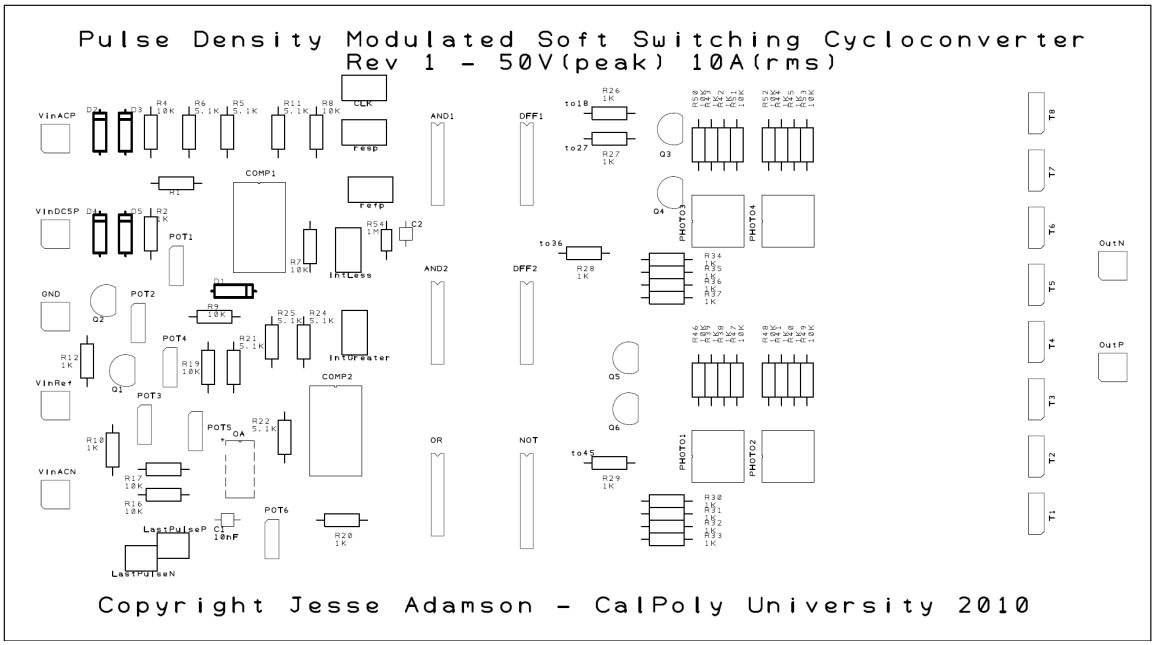

Figure 5-2. PCB Layout: Silkscreen

The copper trace thickness on both layers is 1 ounce (per square foot). Four different trace widths are implemented: the main AC power lines are 0.250 inches wide, the ground plane is 0.050 inches wide, the 5 V power bus is 0.035 inches wide and all signal lines are 0.015 inches wide.

Minimum trace spacing exceeds 0.010 inches. Trace corners are smoothed to 45 degree angles where possible to reduce interference, though this should not be required due to the circuit's relatively low frequency operation. Pairs of extra solder holes have been placed with silkscreen labels to allow easy access to control signals as defined in Table 3-3 and Table 3-4.

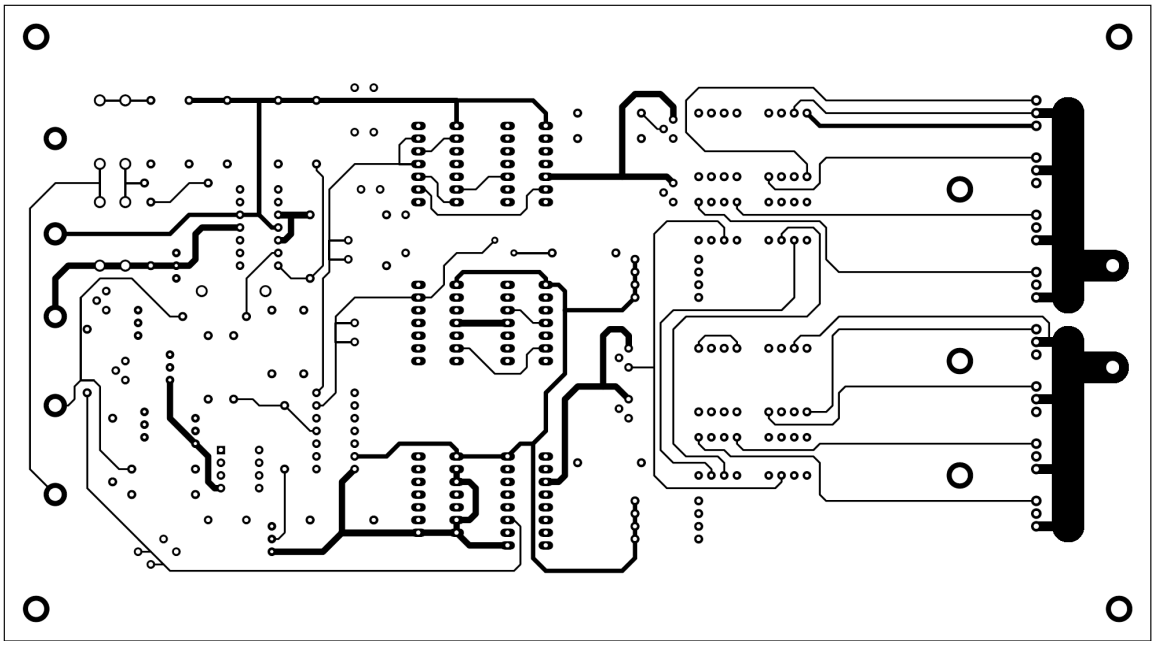

Figure 5-3. PCB Layout: Top Traces

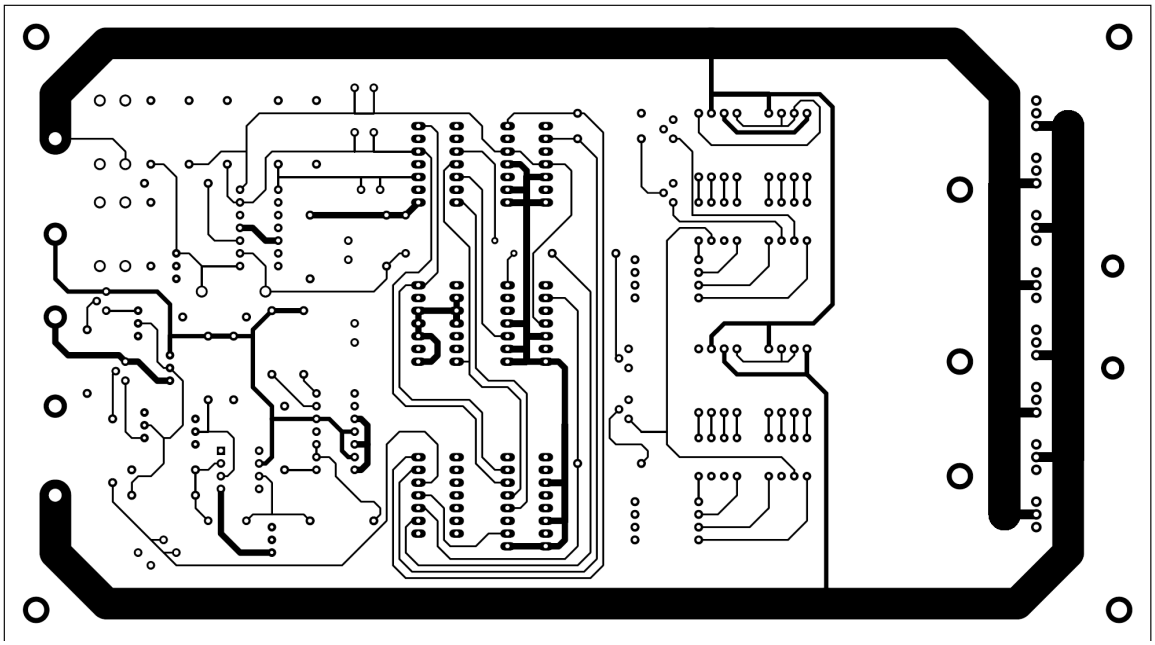

Figure 5-4. PCB Layout: Bottom Traces

The board layout follows the block diagram in Figure 3-7 with power and signal flow from left to right. The left most quarter of the board is the Analog Block, the center left is the Logic Block, the center right is the drivers and the far right is the eight thyristors.

The PCB was produced by Advanced Circuits. Components were ordered from Digikey and Futurlec. IC sockets were used to allow easy removal and replacement of chips. The partially populated circuit board is shown in Figure 5-5.

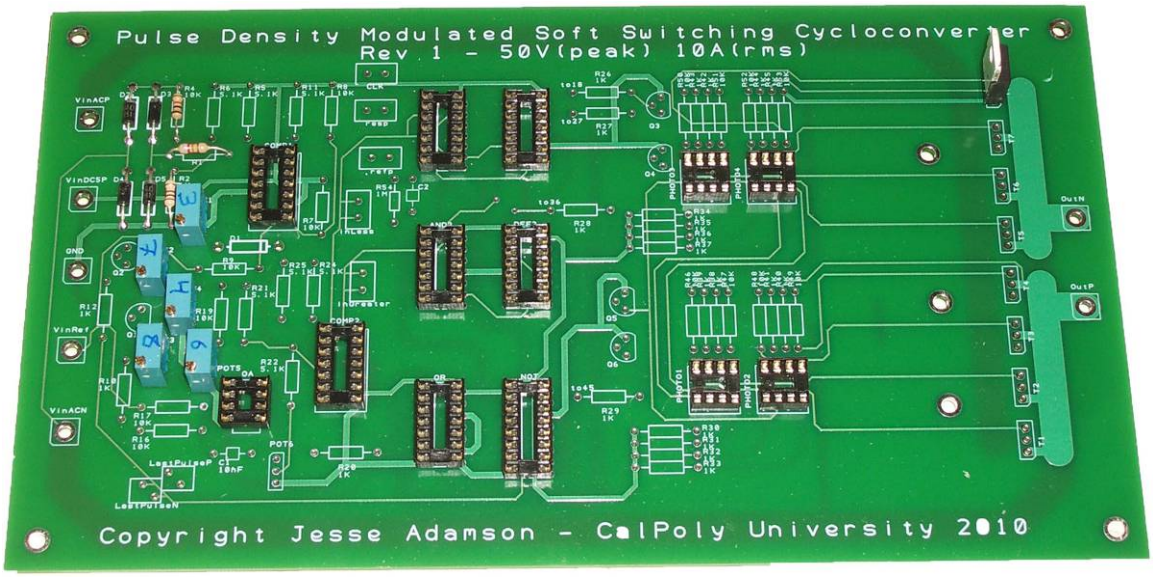

Figure 5-5. PCB Partially Populated

5.2. Test Setup

The soft switching cycloconverter was tested in the Power Electronics Lab at CalPoly. The main AC power supply used was the Invertron 501TC, a 500 VA, variable frequency, isolated AC power supply by California Instruments. Its Series 850T control module was set to a frequency of 5 KHz and an amplitude of 50 volts peak. This was the maximum frequency attainable with this control module.

The GwINSTEK GPM-8212 Power Meter was connected between the Invertron and the cycloconverter input to measure input voltage, current, power and power factor. Additionally, two M9803R True RMS Digital Multimeters were used to sequentially verify the input RMS voltage and RMS current, as well as measure the output RMS voltage and RMS current.

The low voltage control circuitry was powered by 5 VDC from the GwINSTEK GPR-6060D isolated DC power supply. VREF was supplied by the GwINSTEK CFG-3015 Function Generator. This function generator was grounded. It was important that at most one instrument be grounded due to the separation of the high power neutral and signal power ground planes through the diode bridge (Figure 4-11).

Due to the isolation constraints, two portable Fluke 196C Oscilloscopes were used to plot input, output and signal voltage waveforms. The output harmonic content and THD was monitored jointly by the Fluke 43B Power Quality Analyzer and the Power Sight P3000.

Table 5-1. Test Equipment List

Instrument	Qty.	Function
Invertron 501TC	1	Main 50Vp 5KHz AC Power Source
GwINSTEK GPR-6060D	1	5V DC Power Source
GwINSTEK CFG-3015	1	V_{REF} Signal Source
GwINSTEK GPM-8212	1	Measure $I_{IN\text{-}RMS}$, $V_{IN\text{-}RMS}$, P_{IN}, PF_{IN}
M9803R True RMS DMM	2	Measure $V_{OUT\text{-}RMS}$, $I_{OUT\text{-}RMS}$, $V_{IN\text{-}RMS}$, $I_{IN\text{-}RMS}$
Fluke 196C O-Scope	2	Plot Voltage Waveformes
Fluke 43B Pwr. Qlty.	1	Measure output voltage harmonic content
Power Sight P3000	1	Measure output voltage and current THD
GwINSTEK LCR-819	1	Verify inductor and capacitor values

5.3. Calibration

The PCB was populated, calibrated and tested in sections starting with the analog block section in Figure 4-11. After all the components in this section were soldered onto the board, the circuit was energized and the “resp” signal was verified (Figure 5-6). It was noted that the duty cycle of “resp” was slightly above 50%, which is less than ideal.

There are two shortcomings of the “resp” generator circuitry that might contribute to this. One is that the rectifier tap going to “COMP1-2” is not symmetrical. That is, it produces a 50 volts peak positive half cycle, but is clamped to the diode drop (around -0.7 V) for the negative half cycle. The other issue is that this -0.7 V on the negative half cycle is below the ground rail of the comparator. It is within the datasheet specifications, but would not be a good implementation for a production device.

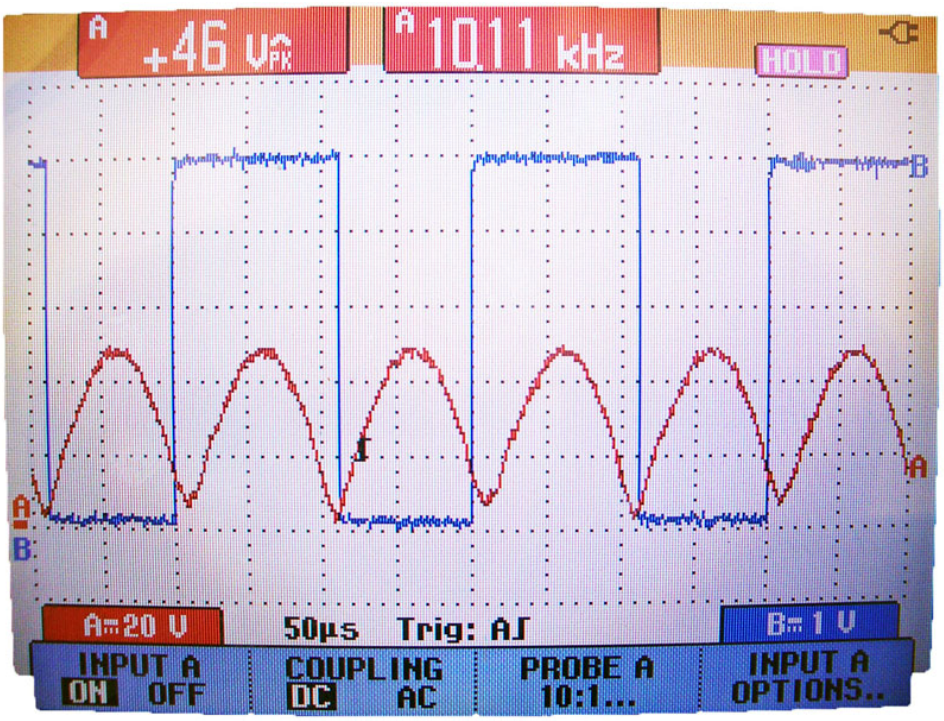

Figure 5-6. "resp" Signal Verification (red is rectified "Vsrc", blue is "resp")

The "CLK" signal is adjusted by "Pot1" which was initially set around 1 KΩ and tuned to produce the waveform in Figure 5-7. This shows the clock rising somewhere in the middle of each half cycle of "Vsrc". This rising edge is when the flipflops change, thereby activating the driving circuitry and priming any necessary reversed biased thyristors to turn on when they become forward biased. "CLK" as well as "resp" compare well to their simulations in Figure 4-2.

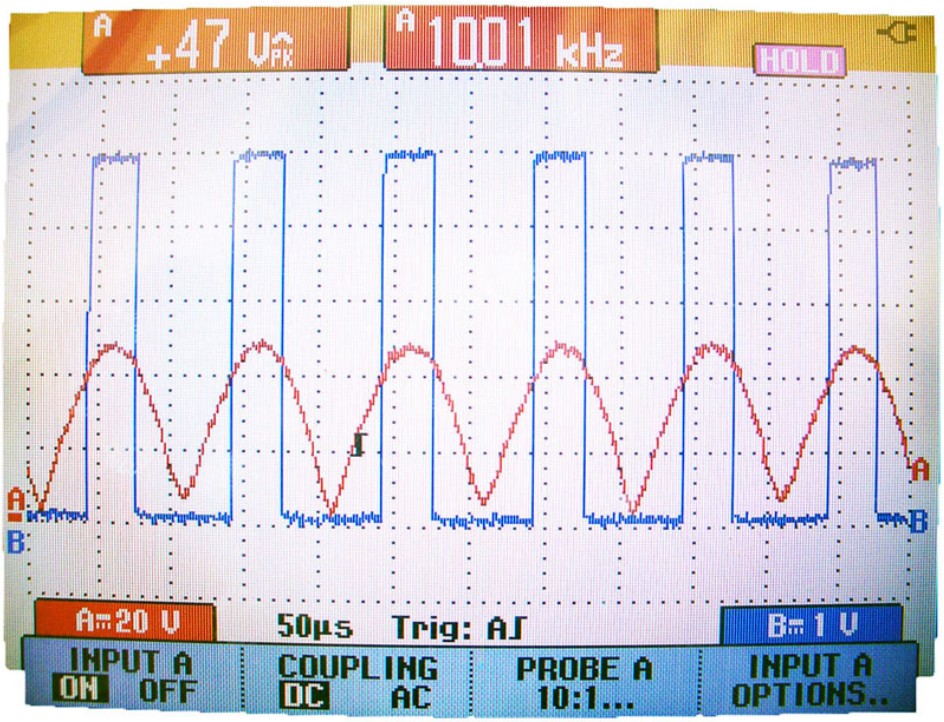

Figure 5-7. "CLK" Signal Verification (red is rectified "Vsrc", blue is "CLK")

After "resp" and "CLK" were verified, the next section of the Analog Block (Figure 4-10) was populated and calibrated. Because the feedback signals "lastPulseP" and "lastPulseN" come from the Logic Block, this section could not be fully calibrated until the Logic Block had been added.

"Pot4" through "Pot6" were calibrated with the DC supply voltage. This involved setting the "Pot4" wiper exactly in the middle so it read 2.5 V. "Pot5" was adjusted to equal "R19" setting the "OA" origin at 2.5 V (half of "VinDC5"). "Pot6" was adjusted to equal "R21". This produced 1.667 V for the "intLess" threshold and 3.336 V for the "intGreater" threshold. "Pot2" and "Pot3" were both set to 2.5 KΩ.

After the Logic Block chips were inserted into their respective sockets, the feedback loop was complete and the rest of the control signals were tested. “refp” is shown in Figure 5-3. This figure shows significant noise in the “refp” signal that appears to be from the “lastPulseP” and “LastPulseN” feedback. This noise level is large enough to produce glitches that could propagate to the output. This noise issue was not solved.

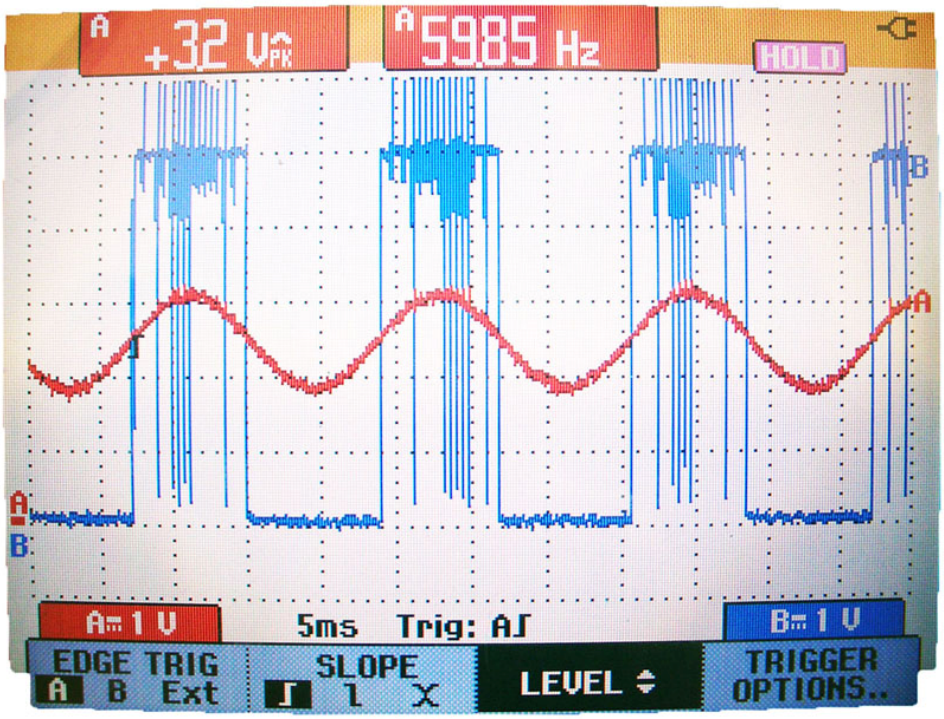

Figure 5-8. “refp” Signal Verification (red is Vref, blue is refp)

Next the integrator signal was calibrated. The integrator is affected by several potentiometer values, however, it was calibrated by exclusively adjusting the amplitude and offset of “Vref”. This was eyeballed to get good symmetry and

tight pulse spacing on the feedback lines “lasPulseP” and “lastPulseN”. The final “VRef” function generator settings were 1.24 Vp-p with a 2.43 V offset at 60 Hz.

The integrator voltage is seen in Figure 5-9 centered on 2.5 V. Each peak in each positive half cycle is evidence of “intGreater” triggering a negative output pulse that is negatively fed back to the integrator through “lastPulseN”. Each valley in each negative half cycle is evidence of “intLess” triggering a positive output pulse that is negatively fed back through “lastPulseP”.

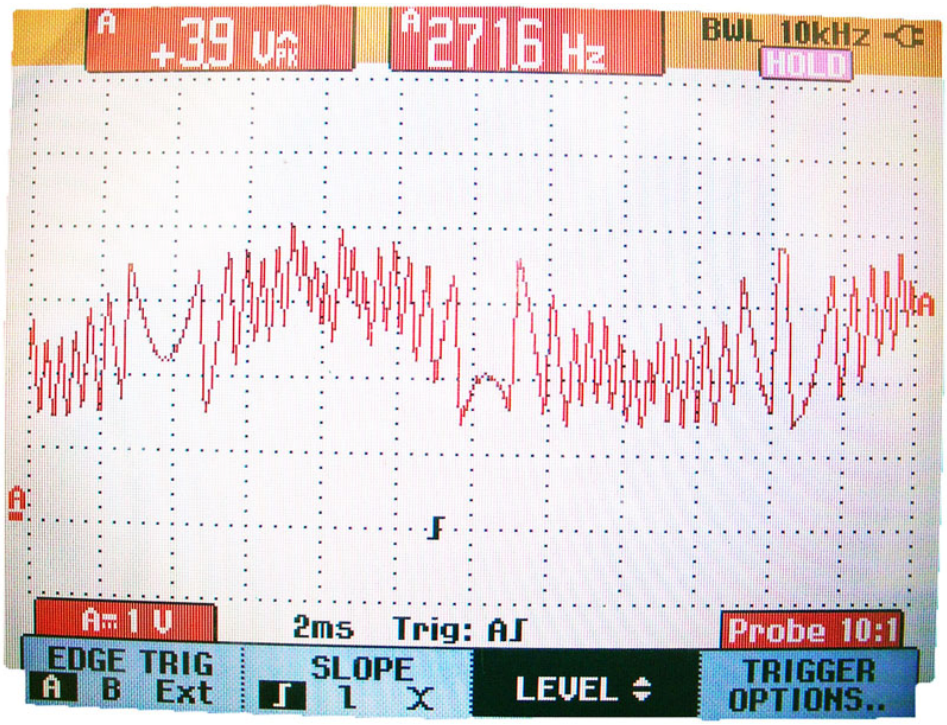

Figure 5-9. Integrator Signal Verification (integrator output voltage to GND)

“lastPulseP” and “lastPulseN” are overlaid on “VRef” in Figure 5-10 and Figure 5-11 respectively. It is noted that “lastPulseP” is active high to drive NFET Q1, while “lastPulseN” is active low to drive PFET Q2.

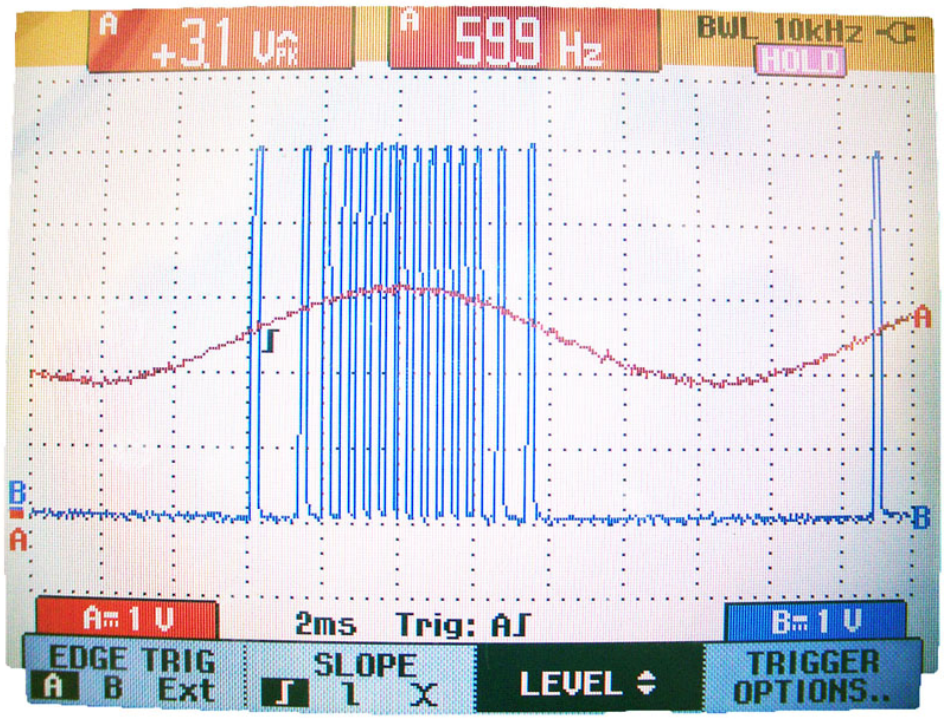

Figure 5-10. “lastPulseP” Signal Verification (red is “VRef”, blue is “lastPulseP”)

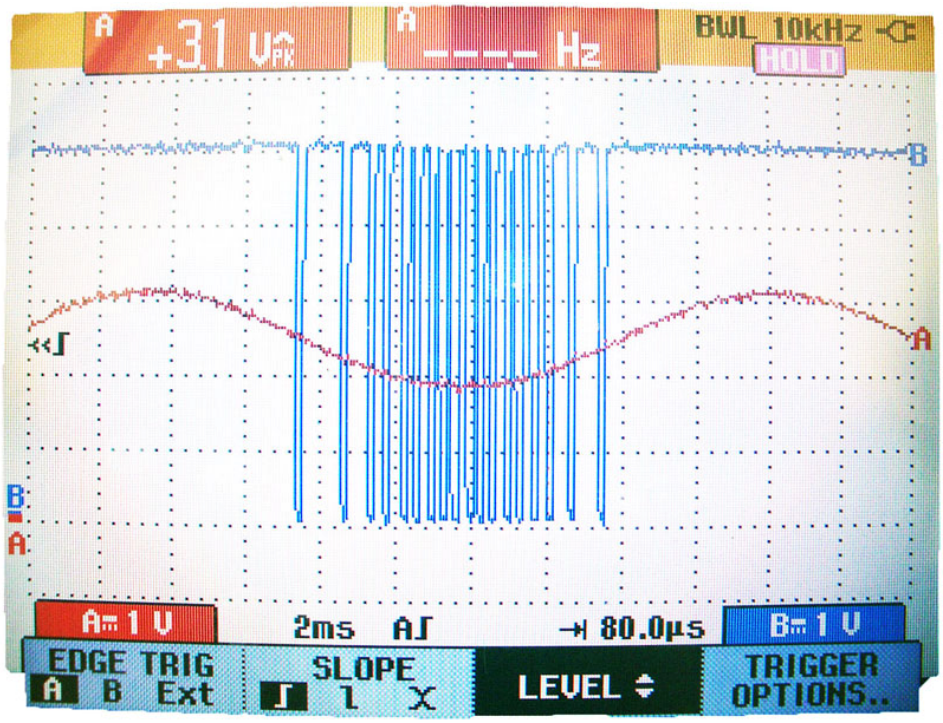

Figure 5-11. “lastPulseN” Signal Verification (red is “Vref”, blue is “lastPulseN”)

The logic block output to the driver circuitry is shown in Figure 5-12. This shows “TO36” and “TO45” which is a 180 degree phase shifted version of “TO18” and “TO27”. Using the integration control scheme, however, causes each half cycle to be unique, with different spacing and polarity pulse lineup (respective number and order of “TO18” and “TO27” pulses or “TO36” and “TO45” pulses).

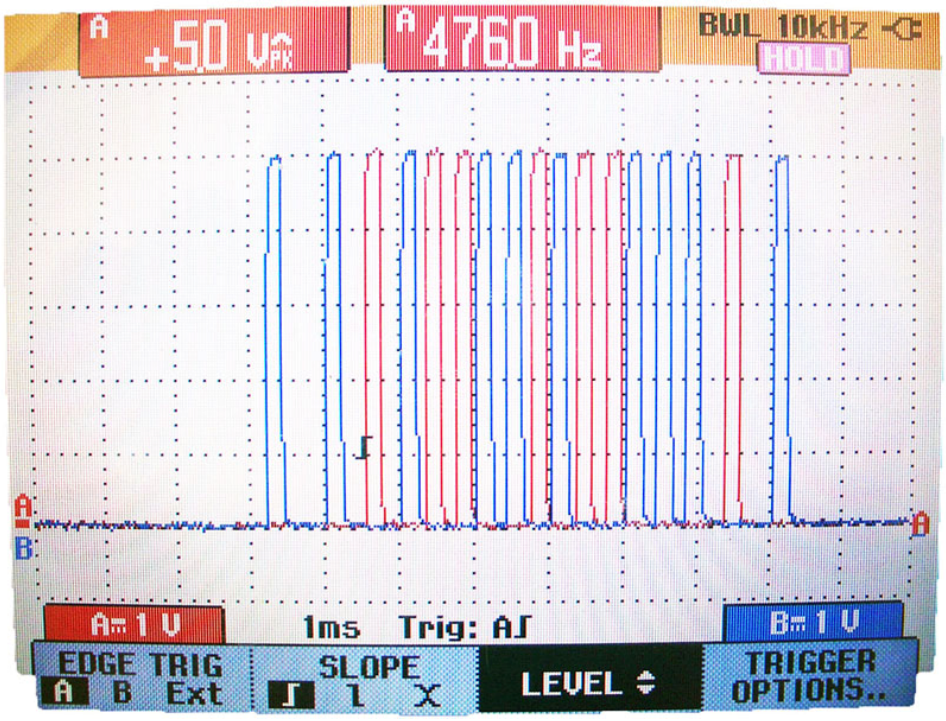

Figure 5-12. Driver Signal Verification (red is “TO36”, blue is “TO45”)

Once the driver signals were in place, the power stage was connected. A piece of ¾ inch aluminum box tube was used for a heat sink. The thyristors were attached to it with an electrical isolated thermal pad and plastic screws to prevent shorting. The final board is shown in Figure 5-13.

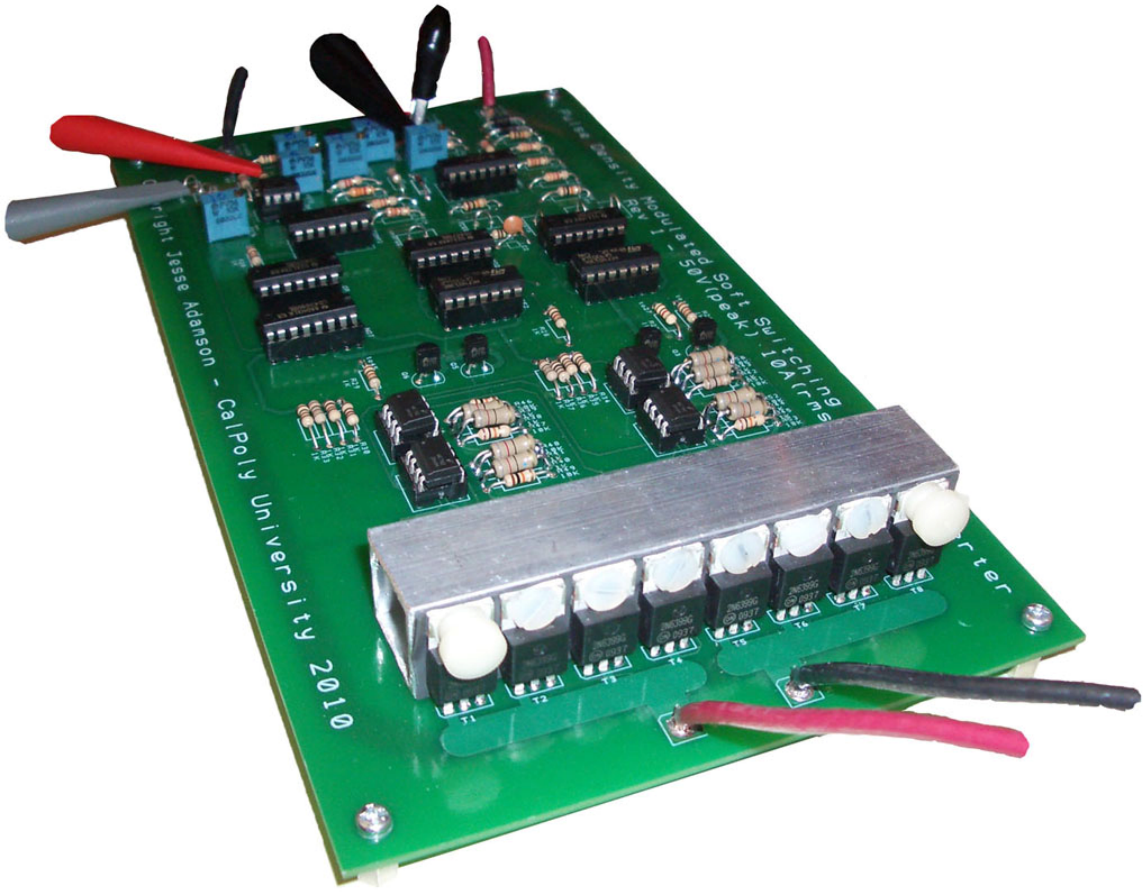

Figure 5-13. Fully Populated PCB Ready for Testing

5.4. Design Changes

There were several issues that required design changes while assembling and calibrating the soft switching cycloconverter. First, the 741 op-amp chip was not able to drive the output to the low voltage threshold of “IntLess” (1.667V). Several chips were tried and all would stop around 2V. This was solved by replacing the 741 with a TL081CN op-amp which easily drove its output well below the threshold.

The PCB was ordered before the final driver circuit was designed. For this reason, the protective zener diodes “D15” through “D22” were not incorporated. The resistor values “R30” through “R37” and “R39” through “R53” were mislabeled on the silkscreen as well.

The zener diodes used were 12 V 5 W rated. These were chosen due to availability, and were soldered on the back side of the board. This was not ideal for heat distribution, however, they were significantly over rated and the board would not be operated for extended periods of time.

The resistor values were experimentally determined with “R30” through “R37” changing to 100 Ω and “R39” through “R53” changing to 82 Ω ½ W. The low value of “R39” through “R53” was required to achieve satisfactorily fast turn on of the thyristors. These resistors, however, along with the zener diodes “D15” through “D22” created several paths between the two input AC power rails that wasted significant power and limited the soft switching cycloconverter continuous run time to under 30 seconds. If the converter ran longer than this, the resistors would become too hot and risk damage. These shortcomings of the driver circuitry probably offer the largest potential for future design improvement.

5.5. Unfiltered Analysis

The loads chosen for testing were six combinations of wire wound power resistors ranging from 5Ω to 50Ω. The input to the unfiltered load showed some distortion (Figure 5-15) with the 50 Ω load and significant distortion (Figure 5-16) with the 5 Ω load. The lower amplitude half cycles occur when the thyristors are triggered and the load is connected. These input waveforms power factor measured 0.82 and 0.51 respectively.

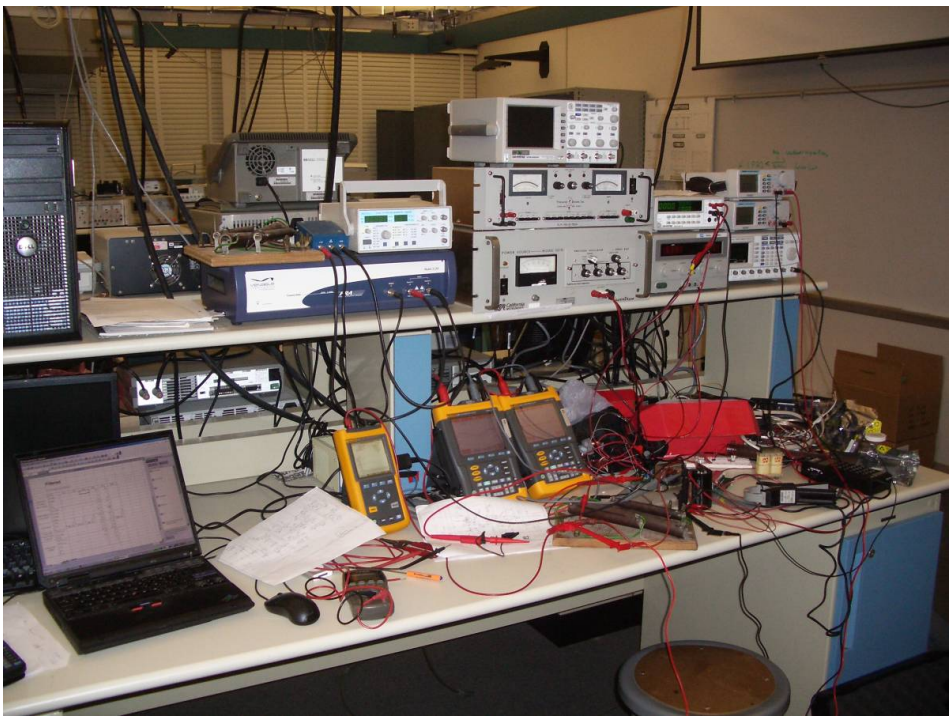

Figure 5-14. Unfiltered Analysis Test Setup

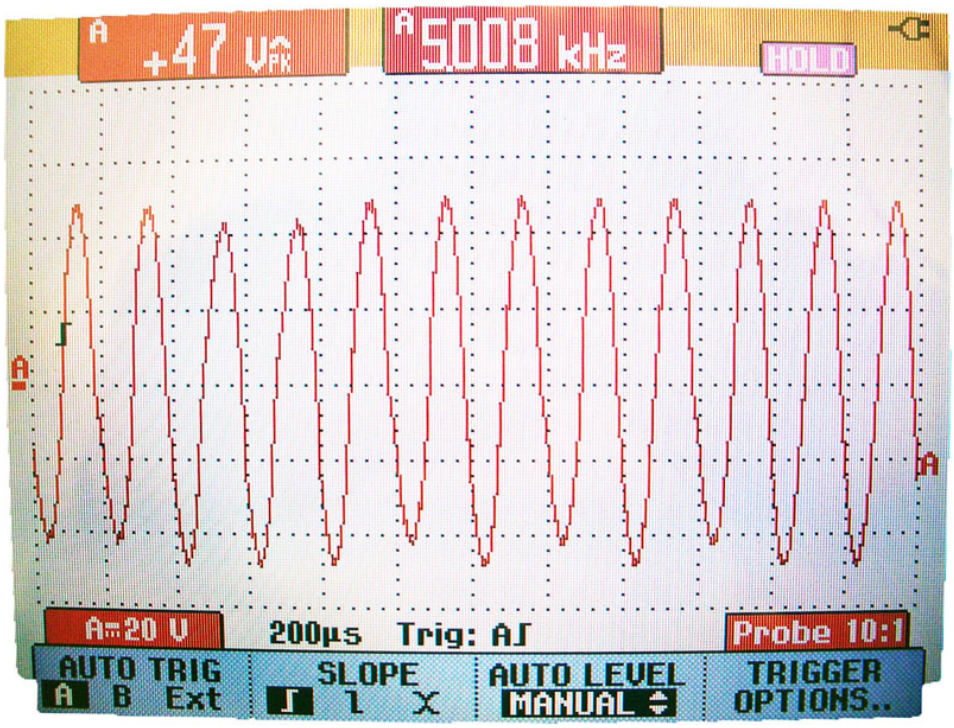

Figure 5-15. Unfiltered Input with R_{LOAD} = 50 Ω

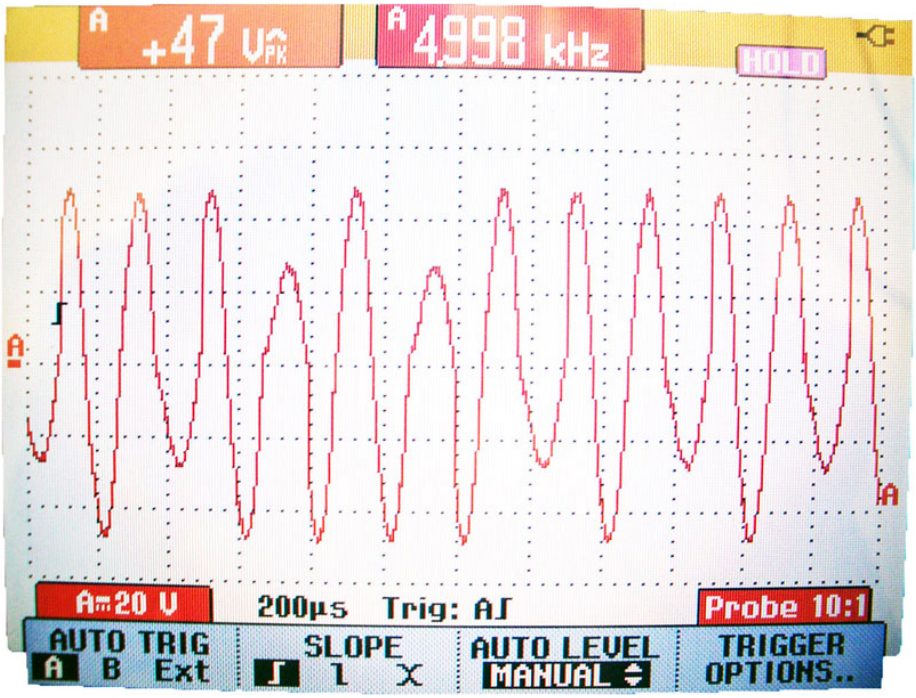

Figure 5-16. Unfiltered Input with R_{LOAD} = 5 Ω

The unfiltered output waveforms for the 50 Ω and 5 Ω load are shown in Figure 5-17 and Figure 5-18 respectively. With the 50 Ω load, the output peaks around 36 V with expected pulse spacing. With the 5 Ω load, however, the peak amplitude drops to 24 V and the pulse spacing reduces. The reduced pulse spacing is signature of a driver malfunction. The pulse density, in this case however, still follows the reference sine wave.

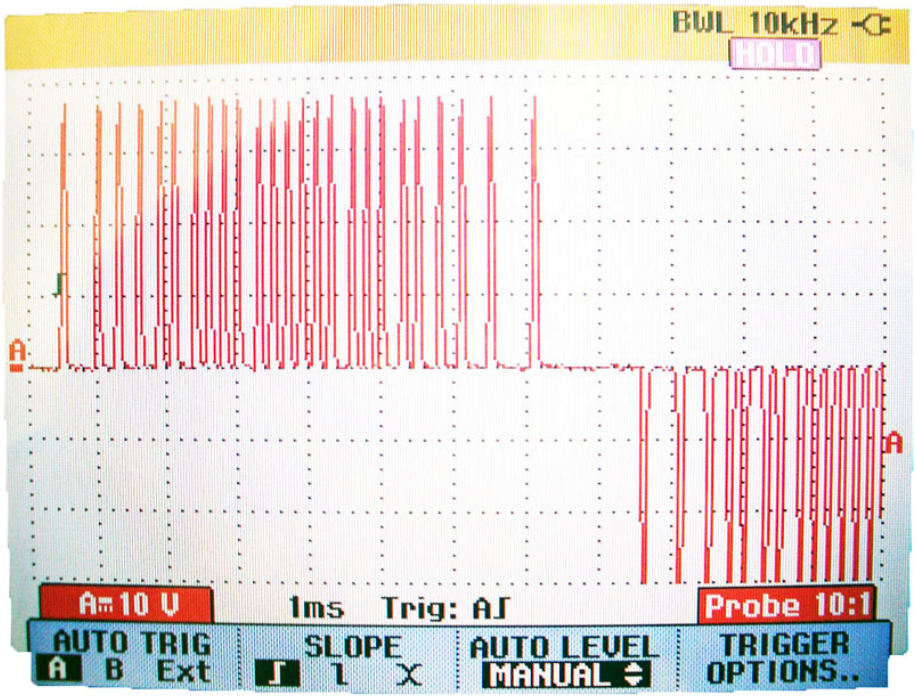

Figure 5-17. Unfiltered Output with R_{LOAD} = 50 Ω

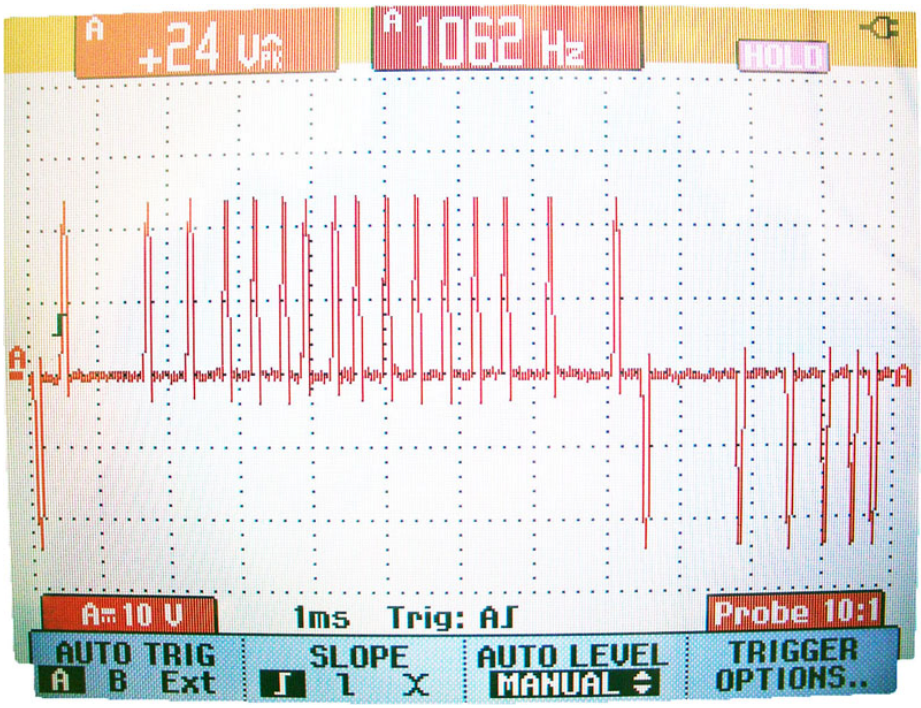

Figure 5-18. Unfiltered Output with R_{LOAD} = 5 Ω

The unfiltered converter was tested and the results are summarized in Table 5-2. The first thing to notice is that the Power Meter gave incorrect readings for the input voltage, which remained 47 V_{PEAK} or 33 V_{RMS} as seen in Figure 5-17 and Figure 5-18. This means that the input power was actually higher than measured, causing the efficiency to be lower than the already low calculated values.

The next thing to notice is the discrepancy between the Fluke and the Power Sight THD measurements. Because the Fluke clearly laid out its results harmonic by harmonic, it is considered more credible in this thesis. Also, the simulation produced a very large harmonic distortion that was more in line with the Fluke. It was further verified that the Fluke was set to THD-F (relative to the

fundamental) as described by equation (3-3). It should be noted that the Fluke only measured the first 50 harmonics, which does not include the 5 KHz input frequency and is therefore significantly lower than the true value. For this reason, the OrCad simulation was set to 50 harmonics as well, and verified to read in THD-F for accurate comparison. The Fluke results are shown in Figure 5-19 and Figure 5-20.

Both the Power Sight and Fluke could measure current as well, but their probes were only accurate to within one amp. For this reason, none of the power sight values are considered accurate in this thesis. The values with "X" depict when the current was too small to register on the Power Sight.

In the "Calculated" section, "$P_{OUT-TOTAL}$" is calculated by multiplying "$V_{OUT-RMS}$" and "$I_{OUT-RMS}$" measured by the true RMS DMM. This is accurate because the inductance of the wire wound resistor is negligible, allowing for the total output power to equal the real output power.

"P_{OUT-1}" is the power of the first harmonic (60 Hz) calculated by multiplying "$P_{OUT-TOTAL}$" by one minus the Fluke "THD(V_{OUT})". The total efficiency "η_{TOTAL}" is calculated by dividing the Power Meter "P_{IN}" by the calculated "$P_{OUT-TOTAL}$". The efficiency of the output considering only the first harmonic "η_1" is calculated by dividing the Power Meter "P_{IN}" by the calculated "P_{OUT-1}"

Table 5-2. Unfiltered Converter Test Results

	LOAD	5Ω	10Ω	15Ω	25Ω	35Ω	50Ω
GwINSTEK GPM-8212 Power Meter	$V_{IN\text{-}RMS}$ (V)	26.6	27.25	27.6	27.5	27.5	27.73
	$I_{IN\text{-}RMS}$ (A)	1.82	1.35	1.13	1.13	1.06	1
	P_{IN} (W)	24.9	23.4	21.86	23.7	23.6	22.8
	PF_{IN}	0.51	0.635	0.7	0.759	0.8	0.824
DMM M9803R (True RMS)	$V_{OUT\text{-}RMS}$ (V)	8.53	10.43	11.5	15.35	16.36	17.07
	$I_{OUT\text{-}RMS}$ (A)	1.54	0.98	0.72	0.57	0.43	0.24
Fluke 43B Power Quality Analyzer	THD(V_{OUT})	75.0%	87.6%	85.1%	42.6%	32.9%	32.1%
	$V_{OUT\text{-}RMS}$ (V)	4.52	5.86	6.3	8.09	9.12	9.32
	$Freq_1$ (Hz)	61.55	61.29	61.17	59.97	60.34	60.34
Power Sight P3000	THD(V_{OUT})	17%	24%	15%	14%	9%	14%
	THD(I_{OUT})	20%	20%	20%	17%	12%	X
	V_{OUT} (V)	4.1	5.1	5.1	5.9	7.4	7
	I_{OUT} (A)	1.3	1	0.7	0.5	X	X
	P_{OUT} (W)	5.8	3.6	2.4	3.1	X	X
Calculated	$P_{OUT\text{-}TOTAL}$ (W)	13.1	10.2	8.3	8.7	7.0	4.1
	$P_{OUT\text{-}1}$ (W)	3.3	1.3	1.2	5.0	4.7	2.8
	η_{TOTAL}	53%	44%	38%	37%	30%	18%
	η_1	13%	5%	6%	21%	20%	12%

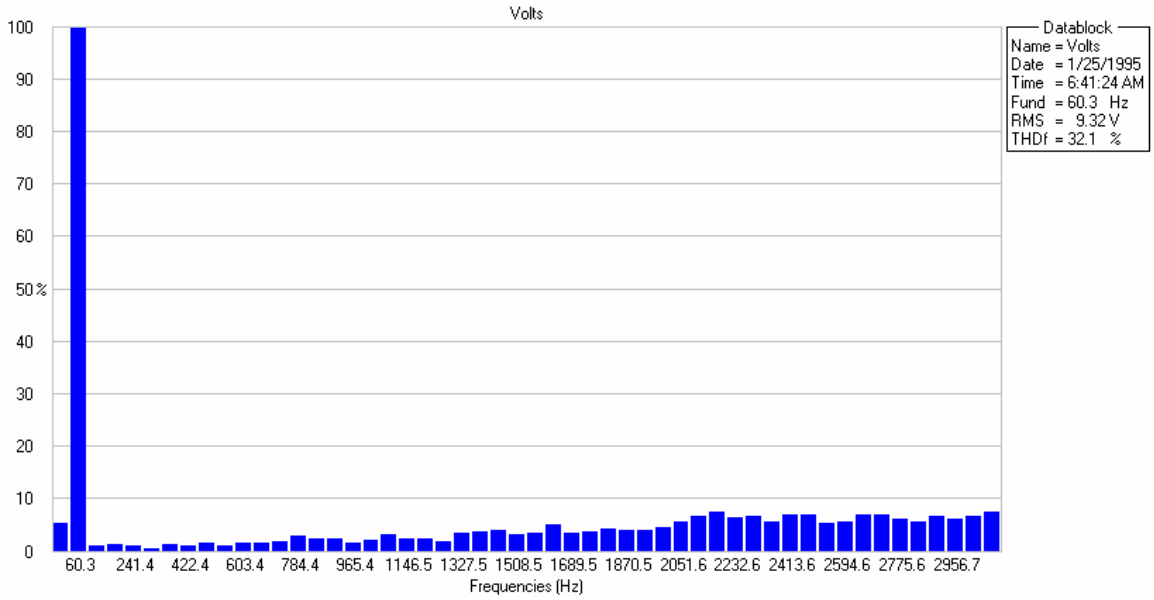

Figure 5-19. Voltage Harmonic Content of Unfiltered Output with 50 Ω Load

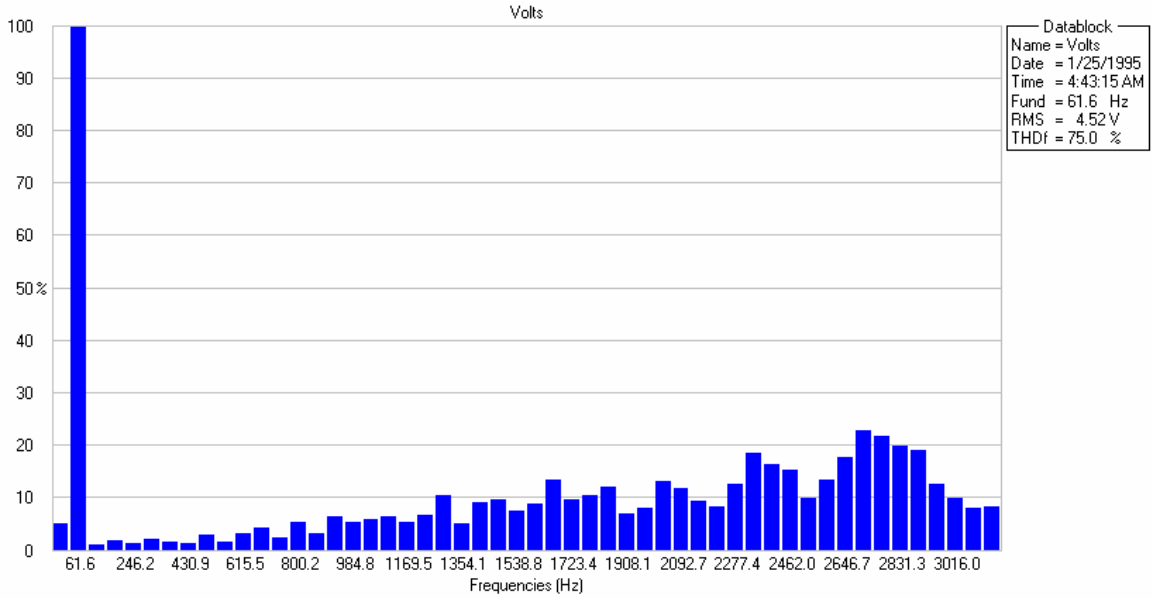

Figure 5-20. Voltage Harmonic Content of Unfiltered Output with 5 Ω Load

5.6. Filtered Analysis

The filter was chosen as the best combination of several of inductors and capacitors for a 25 Ω load. 25 Ω was chosen as a low load value to reduce possible damage to the converter while trying different filters. Also, it was suggested by the filter calculations in Table 3-5 that a lower load would require more filtering. This turned out to be incorrect.

The AC capacitor choices were 158 uF and 30 uF. The inductor choices were 17.4 mH, 18.5 mH, 40 mH, 94 mH and 483 mH. The best choice for a compromise of THD and amplitude came with the 158 uF capacitor and the 18.5 mH inductor and is shown in Figure 5-22 with 8% THD and amplitude 15 V_{PEAK}.

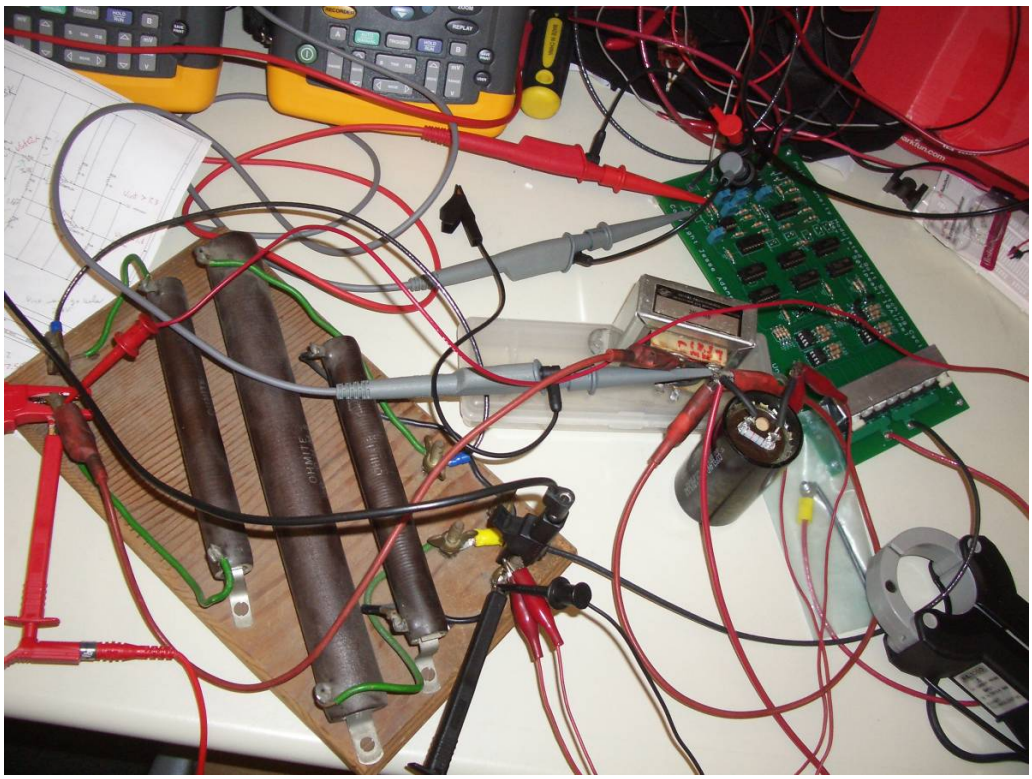

Figure 5-21. Filtered Output Test Setup

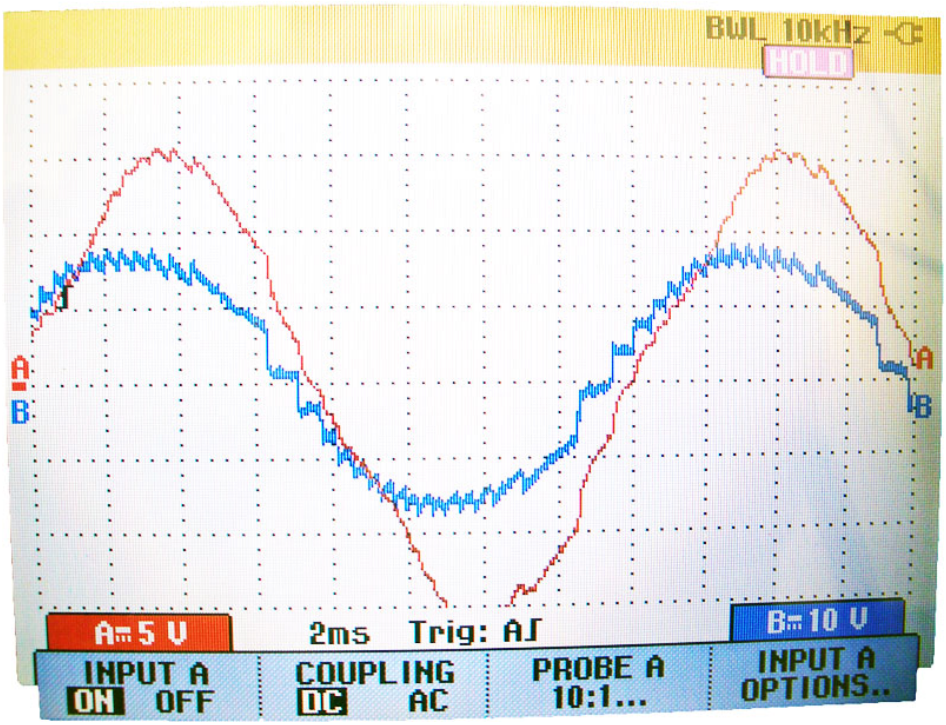

Figure 5-22. Filtered V_{OUT} with 25 Ω Load (red across load, blue across filter)

The output with the 5 Ω load is shown in Figure 5-23. This waveform has 25% THD. This suggests that a larger load requires more filtering, which on one hand seems intuitive but on the other hand contradicts Table 3-5. The contradiction is probably due to the neglecting of power supply output impedance variations. The input for the same load is shown in Figure 5-24 which is significantly worse than the unfiltered input, reducing the power factor to 0.36.

The filtered output test results are summarized in Table 5-3. The first thing to notice is, once again, the low Power Meter input voltage readings. To compensate for this, the true RMS meter was used to verify voltage and current in the input as well, showing significantly higher values for both.

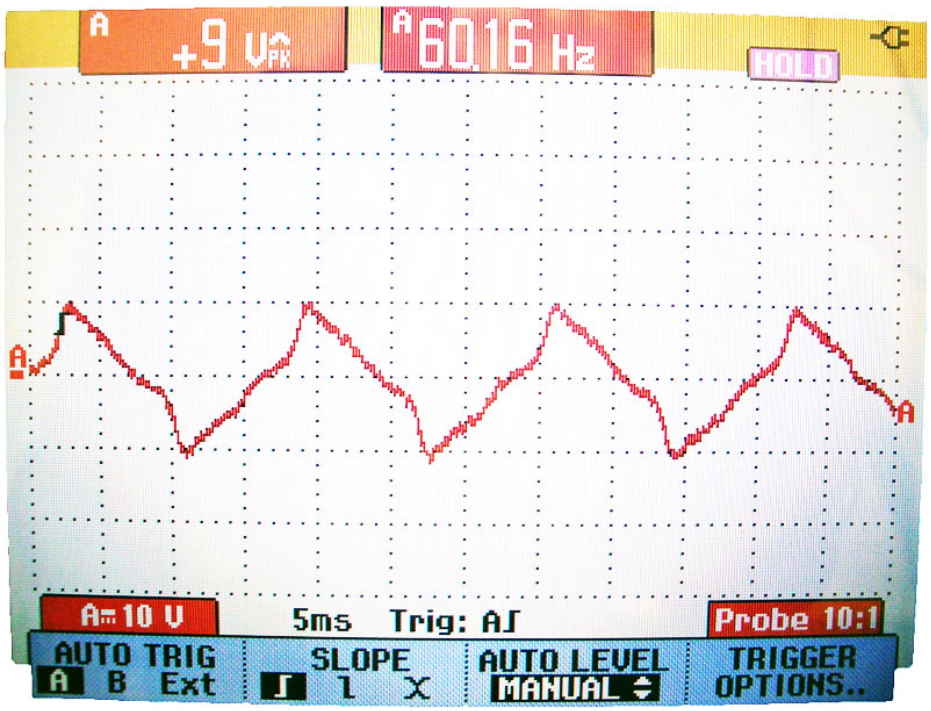

Figure 5-23. Filtered output with 5 Ω Load

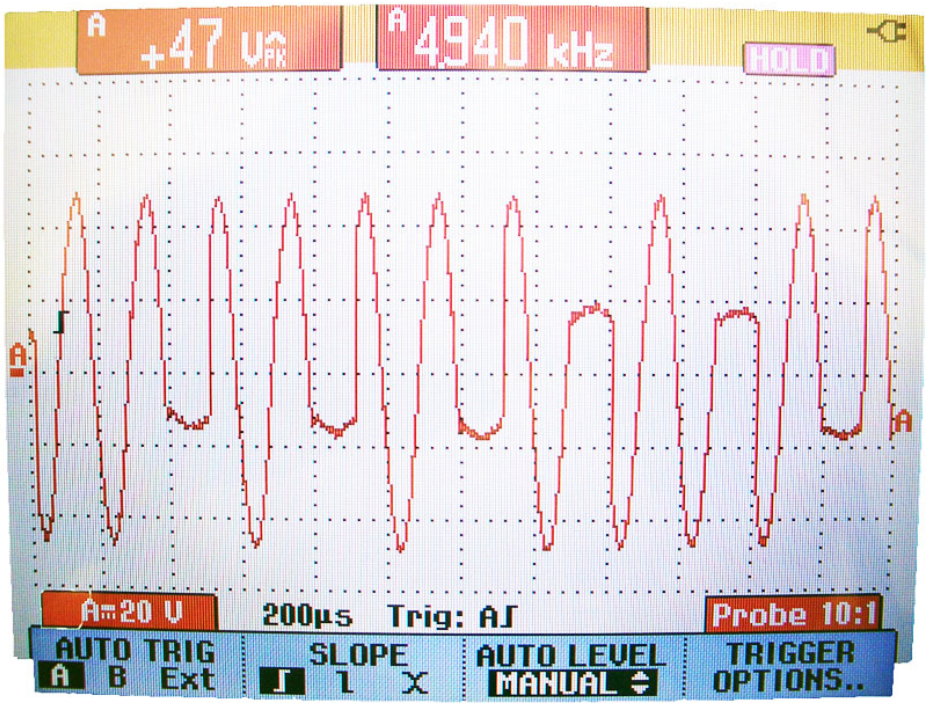

Figure 5-24. Filtered Input with 5 Ω Load

Another strange thing about the filtered results is the relatively constant RMS input and output current for the converter over the entire load range. This attributes to higher power at low loads, increasing low load efficiency. Part of this is accounted for by the filters rejection of power at higher loads due to more harmonic content. This may also be due in some part to a constructive disruption of the inefficient control circuitry that normally wastes several watts of power.

"VA_{IN}" was calculated by multiplying the true RMS DMM "V_{IN}" and "I_{IN}" values by each other. "P_{IN}" is calculated by multiplying "VA_{IN}" by the power "PF_{IN}". "$P_{OUT\text{-}TOTAL}$" was calculated by multiplying "$V_{OUT\text{-}RMS}$" by "$I_{OUT\text{-}RMS}$". $P_{OUT\text{-}1}$" was found by multiplying "$P_{OUT\text{-}TOTAL}$" by one minus the Fluke "THD(V_{OUT})". The total efficiency "η_{TOTAL}" is calculated by dividing "$P_{OUT\text{-}TOTAL}$" by "P_{IN}". The efficiency including only the output power of the first harmonic "η_1" is found by dividing "$P_{OUT\text{-}1}$" by "P_{IN}".

Table 5-3. Filtered Converter Test Results

	LOAD	5Ω	10Ω	15Ω	25Ω	35Ω	50Ω
GwINSTEK GPM-8212 Power Meter	$V_{IN\text{-}RMS}$ (V)	25.7	25.8	26	26.2	26.1	26
	$I_{IN\text{-}RMS}$ (A)	2.25	2.1	2.1	2.1	2.1	2.14
	P_{IN} (W)	21.6	21.5	21.6	21	21	20.1
	PF_{IN}	0.357	0.38	0.39	0.38	0.39	0.36
DMM M9803R (True RMS)	$V_{OUT\text{-}RMS}$ (V)	5.38	7.74	9.1	10.56	10.51	12.2
	$I_{OUT\text{-}RMS}$ (A)	2.36	2.16	2.12	2.13	2.13	2.2
	$V_{IN\text{-}RMS}$ (V)	34.58	35.75	35	34.26	35.15	35.96
	$I_{IN\text{-}RMS}$ (A)	2.53	2.36	2.32	2.33	2.31	2.35
Fluke 43B Power Quality Analyzer	$THD(V_{OUT})$	25.1%	15.5%	11.4%	8.1%	8.0%	6.9%
	$V_{OUT\text{-}RMS}$ (V)	5.34	7.72	9.05	10.36	10.45	12.15
	$Freq_1$ (Hz)	59.97	59.97	60.1	60.04	60.04	60.1
Power Sight P3000	$THD(V_{OUT})$	25%	16%	11%	9%	8%	8%
	$THD(I_{OUT})$	38%	45%	32%	47%	52%	32%
	V_{OUT} (V)	5.4	7.7	9.2	10.7	10.6	12.3
	I_{OUT} (A)	1.6	1.9	1.9	1.7	2.5	1.9
	P_{OUT} (W)	3.7	3	3.8	3.1	3	0.1
Calculated	VA_{IN} (VA)	57.83	54.18	54.6	55.02	54.81	55.64
	P_{IN} (W)	31.2	32.1	31.7	30.3	31.7	30.4
	$P_{OUT\text{-}TOTAL}$ (W)	12.7	16.7	19.3	22.5	22.4	26.8
	$P_{OUT\text{-}1}$ (W)	9.5	14.1	17.1	20.7	20.6	25.0
	η_{TOTAL}	41%	52%	61%	74%	71%	88%
	η_1	30%	44%	54%	68%	65%	82%

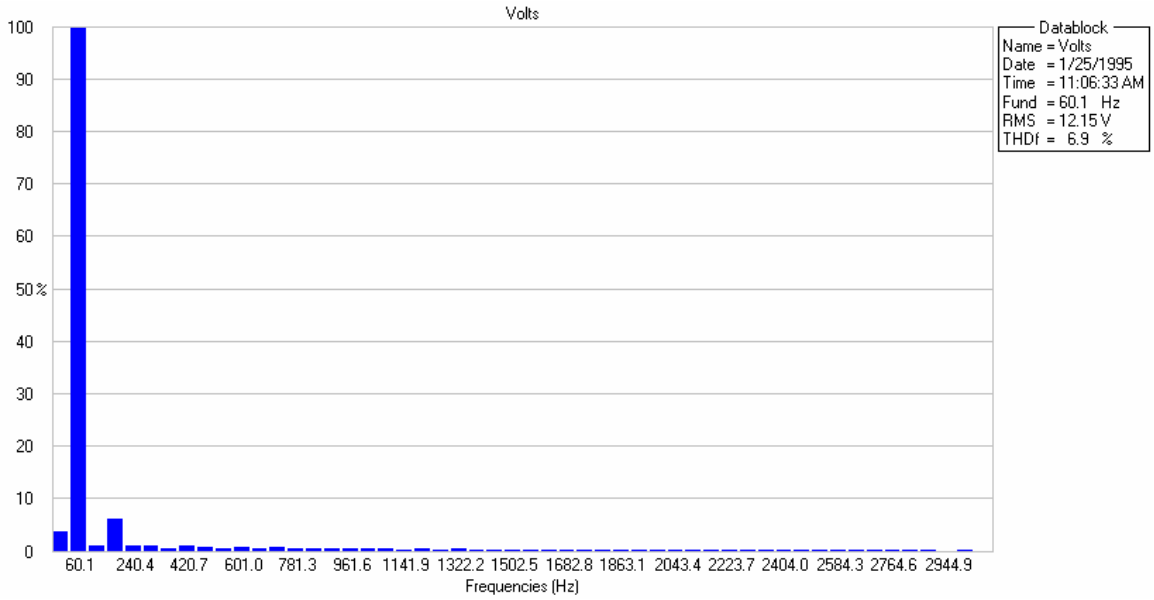

Figure 5-25. Voltage Harmonic Content of Filtered Output with 50 Ω Load

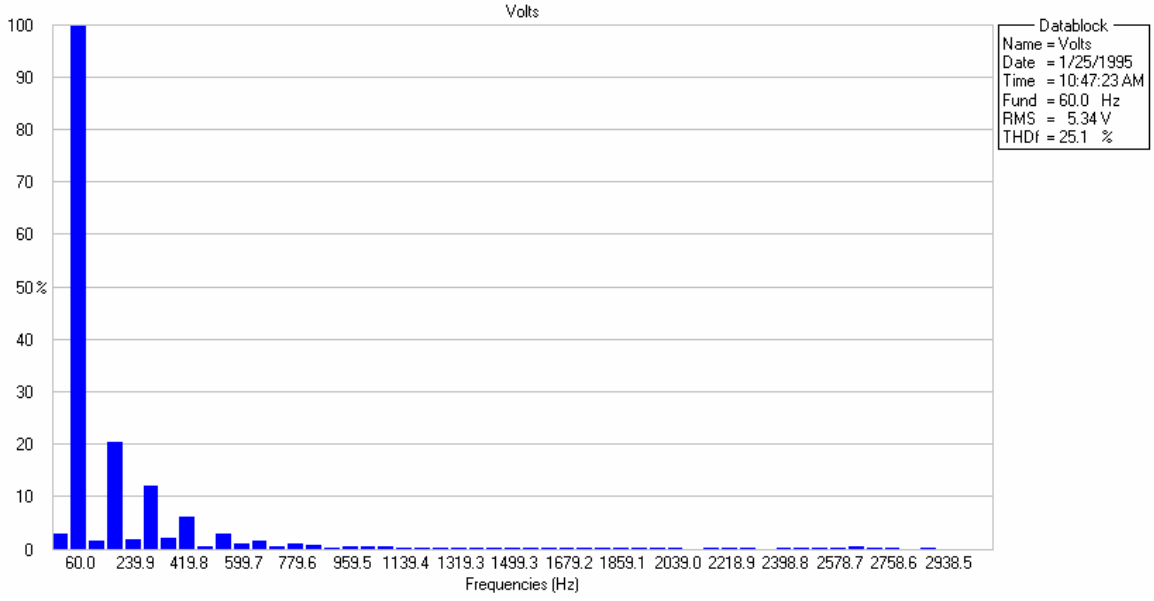

Figure 5-26. Voltage Harmonic Content of Filtered Output with 5 Ω Load

5.7. Soft Switching

The switching trajectory is shown in Figure 5-27 for the unfiltered 5 Ω load and in Figure 5-28 for the filtered 5 Ω load. The blue lines are voltage across thyristors T1 and T3 (they are in parallel). The pink lines are voltage out of the positive thyristor node, the one containing T1, T2, T3 and T4. For the unfiltered load, the first full current pulse (from left to right) does not go through the switch under test (T1 or T2) and so there is a full voltage pulse with only a slight distortion bend visible. The second and third current pulses coincide with near zero voltage flat lines. This is the signature of zero voltage and current turn on and turn off.

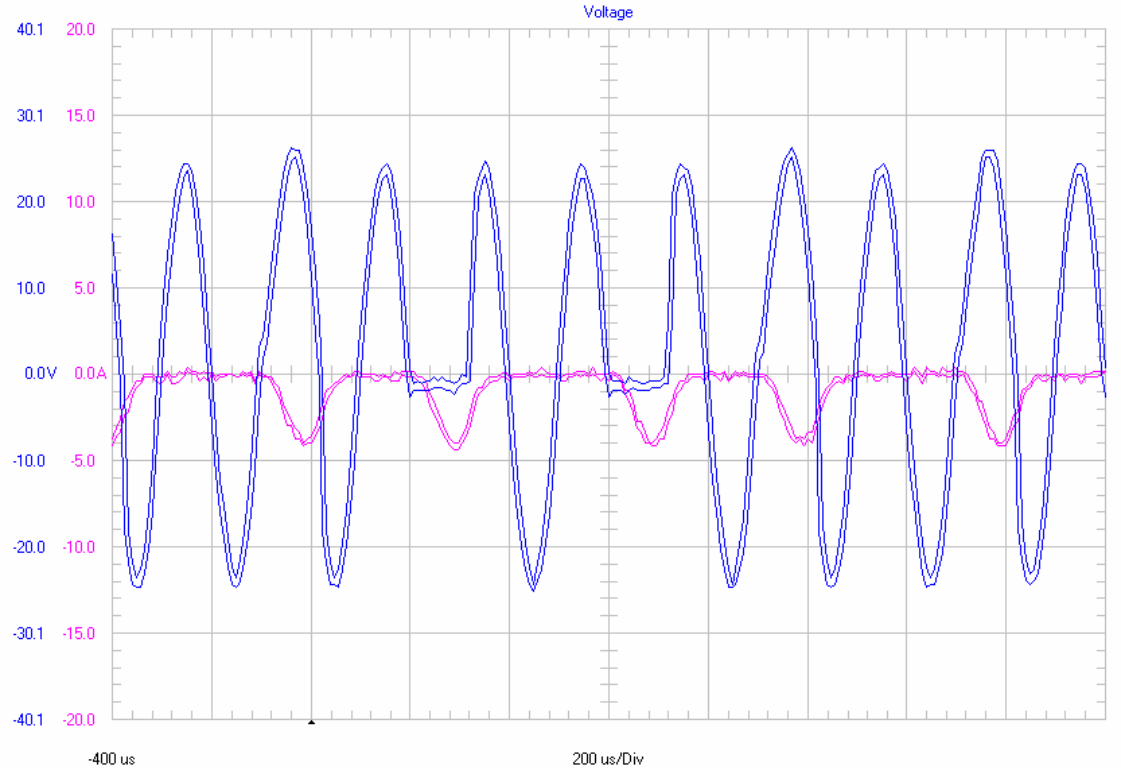

Figure 5-27. Switching Trajectory Unfiltered with 5 Ω Load (blue is V, pink is I)

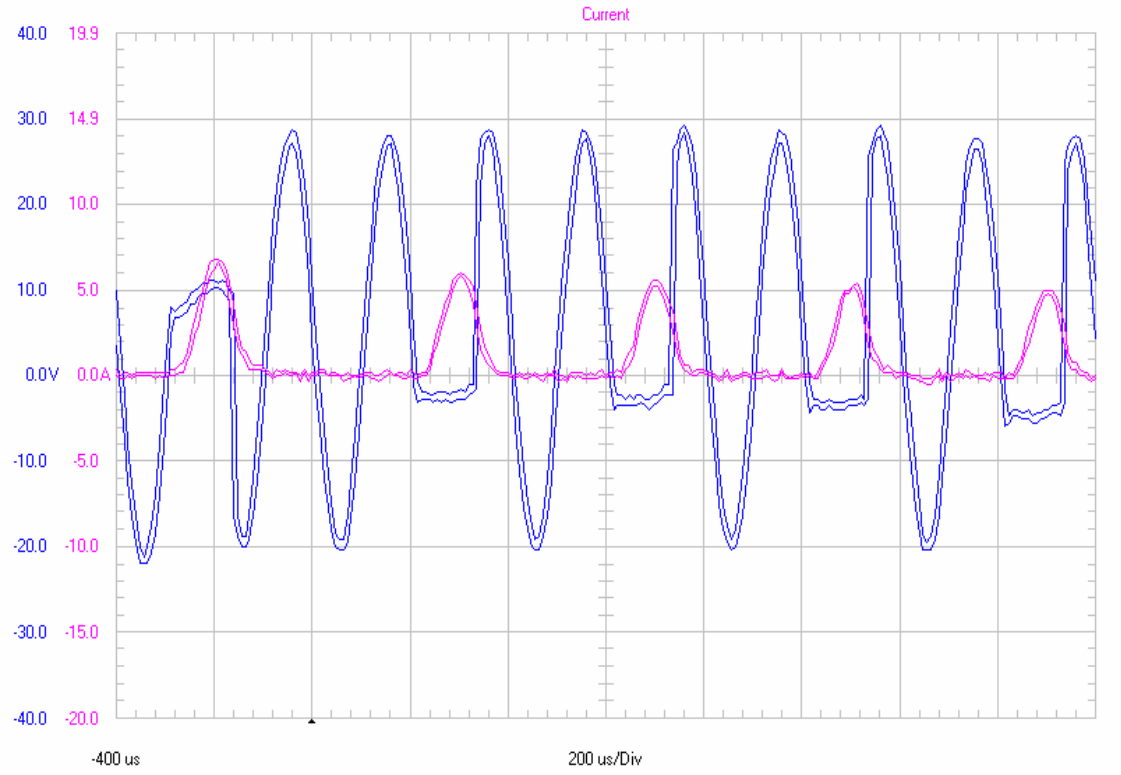

Figure 5-28. Switching Trajectory Filtered with 5 Ω Load (blue is V, pink is I)

Looking closer, however, the voltage turn off is not exactly soft. The current drop is shifted too far to the left of the voltage rise, and the voltage rises too steeply. This is due to the long reverse recovery time issue seen in the OrCad simulation. This problem is accentuated in the filtered case. The best solution to this would be a switch with faster turn off.

This converter topology had been tested, with some interesting results that entice further study. Several weaknesses have been identified that could greatly improve performance, such as thyristor driver circuitry, filter design and input power factor. These strengths and weaknesses, as well as future opportunities for study, will be further discussed in the following chapter.

Chapter 6. Conclusion

In this thesis a soft switching cycloconverter has been hypothesized, simulated, prototyped and tested. On the surface, this topology appeared to have the advantage of reducing switching losses compared to standard cycloconverters, allowing it to operate at higher frequencies. This is important for very high frequency to low frequency conversion applications, such as reducing the frequency of resonant inverters to a more manageable level for grid applications or motor drives.

There is a tradeoff however, because the switching losses were reduced by employing soft switching at turn on (a cycloconverter already has soft switching at turn off) which requires letting entire half cycles of the input waveform through to the load. This results in the requirement of a very large input frequency to output frequency ratio (the minimum should be closer to 100, as apposed to 3 in a standard cycloconverter).

The prototype left much to be desired. The simulations were promising, but had several shortcomings of their own. First, there was a severe discrepancy between filter requirements in original calculations, the Simulink model and the OrCad PSpice model. The Simulink model actually correlated better with actual hardware filtering observations, even though the OrCad PSpice model used more extensive and specific device models.

First, on the signal side, “CLK” worked. However, it could be improved by narrowing the clock pulse to get the rising transitions closer to the peaks of the

input signal. Second, the resp signal was a little asymmetrical, and probably one cause of the slight DC offset seen in the harmonic breakdowns Figure 5-19, Figure 5-20, Figure 5-25 and Figure 5-26. The “refp” signal was very symmetric, but had significant noise that could be attributing to output anomalies. It would help to better isolate this signal from the feedback “lastPulseP” and “lastPulseN”.

The hardware switches, though implemented with a non-standard heat sink, did not warm up noticeably during testing. This is surprising considering the OrCad model suggested they’d have 37 W of power dissipation with no filter, and a ridiculously large 5.6 KW of power dissipation with the large filter in Figure 4-26.

The driver circuitry was arguably the largest shortcoming of this design. This could be easily improved and significantly increase efficiency. The simplest fix would be to swap out the BJT photocouplers for devices with larger forward and significantly larger reverse blocking capabilities, such as thyristor or triac photocouplers. This would allow the elimination of the zener diodes, reducing the loss by a simulation estimated 700 mW.

Swapping out the photocouplers would also greatly reduce the current in “R39” through “R45”, and possibly allow eliminating these resistors all together. This could work well since by shorting the gate to the anode, the thyristors should turn on as fast and softly as possible. The soft turn on should automatically limit the gate cathode current, and once the thyristor turned on, its low voltage drop would continue the same limiting effect.

Eliminating “R39” through “R45” would eliminate an unfiltered simulation estimated 18.7 W of power. Calculated from the filtered prototype results, its 14.0 W to 15.7 W depending on the load with a 12 Vrms to 12.7 Vrms drop measured across these resistors. These power comparisons are summarized in Table 6-1.

Table 6-1. Converter Power Distribution at 5 Ω Load

	Simulation Unfiltered	Simulation Filtered	Prototype Unfiltered	Prototype Filtered
Power In (W)	242.5	6145	24.9	31.2
Load Power (W)	182.6	187	13.1	12.7
Switch Power (W)	37	5753	X	X
Zener Power (W)	0.7	0.8	0.8	0.8
Driver R power (W)	18.7	18.7	14.0	14.0
Other Power (W)	3.5	185.5	X	X
Efficiency (%)	75	3	53	42

One thing to notice from Table 6-1 is the incorrectly large powers for the filtered simulation. Once again, this was due to the large filter capacitor shorting 60 Hz current. Another noteworthy issue is the order of magnitude discrepancy between the simulated input and output power and the actual input and output power. This is likely due in part to the added resistance of all the test cables, as well as the high frequency power supply whose resistance is evidenced in Figure 5-16 and Figure 5-24. However, this discrepancy is probably predominantly caused by the lower pulse density anomaly observed at full load in Figure 5-18.

The “Unfiltered Prototype” “Power In” is less than the total of the power losses. This is due to inaccuracies in the power meter used in this measurement. This was adjusted using a combination of true RMS DMM’s to measure RMS voltage and current, along with the power meter to measure power factor in the “Filtered Prototype” case. This calculated out at around 40% more power than the original power meter reading. Likewise, the “Unfiltered Prototype” “Power In” should be closer to the “Filtered Prototype” “Power In”.

The prototype switch losses were not easily measurable. The combined Switch and Other Power totaled 3.7 W for the “Filtered Prototype”, most of which is attributable to switching loss.

Table 6-2. Summary of Specifications for Filtered Converter with 5 Ω Load

Parameter	Input/Line	Output/Load
Number of Phases (ϕ)	1	1
Frequency (Hz)	5000	60
Voltage AC sine (V-Peak)	50	9
Full Load Current AC sine (A-RMS)	N/A	2.36
Regulation (%)	N/A	79
Power Factor	0.357	1
Voltage Frequency Response	N/A	Figure 5-26
Total Harmonic Distortion (%)	N/A	25
Efficiency (%)	42	

The load regulation of this converter rang in at a terrible 79%. This probably has a lot to do with the anomalous drop in pulse density with higher load (Figure 5-18). The input power factor of 0.357 wasn't great either. The 25% THD at full load (5 Ω) was not amazing, but could easily be fixed with a larger output filter. These results are summarized in Table 6-2.

Ultimately, this converter needs a lot more work. The controls need more noise reduction and some revamping to correct the pulse density reduction anomaly. The thyristor driver circuitry needs a huge efficiency boost. The thyristors need help turning off faster. The filter needs a thorough optimal design targeting full load. The converter needs a higher frequency power supply, hopefully one that can better keep up with the short high current pulses.

Eventually, an advanced controller would need to be developed to allow for line regulation. A better controller with actual output feedback may be required as well to boost load regulation. The bad power factor may not be a problem depending on the application.

This thesis has just hit the tip of the proverbial soft switching cycloconverter iceberg. Though there is much work to be done in this area, the doors are now wide open. The problems that have been uncovered are far from insurmountable. Some relative of this control scheme should surely show promise as soft switching transitions to mainstream and power density in power converters continues to rise by increased switching frequency.

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